DATA SHEET

旭曜科技 ORISE TECH

OTM3225C

720-channel 6-bit source driver and 320-channel gate driver with System-On-Chip (SOC) for color amorphous TFT LCD

Preliminary

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720-channel 6-bit source driver and 320-channel gate driver with System-On-Chip (SOC) for color amorphous TFT LCD

1. GENERAL DESCRIPTION

The OTM3225C, a 262144-color System-on-Chip (SoC) driver LSI designed for small and medium sizes of TFT LCD display, is capable of supporting up to 240xRGBx320 in resolution which can be achieved by the designated RAM for graphic data. The 720-channel source driver has true 6-bit resolution, which generates 64 Gamma-corrected values by an internal D/A converter.

The OTM3225C is able to operate with low IO interface power supply up to 1.65V and incorporate with several charge pumps to generate various voltage levels that form an on-chip power management system for gate driver and source driver.

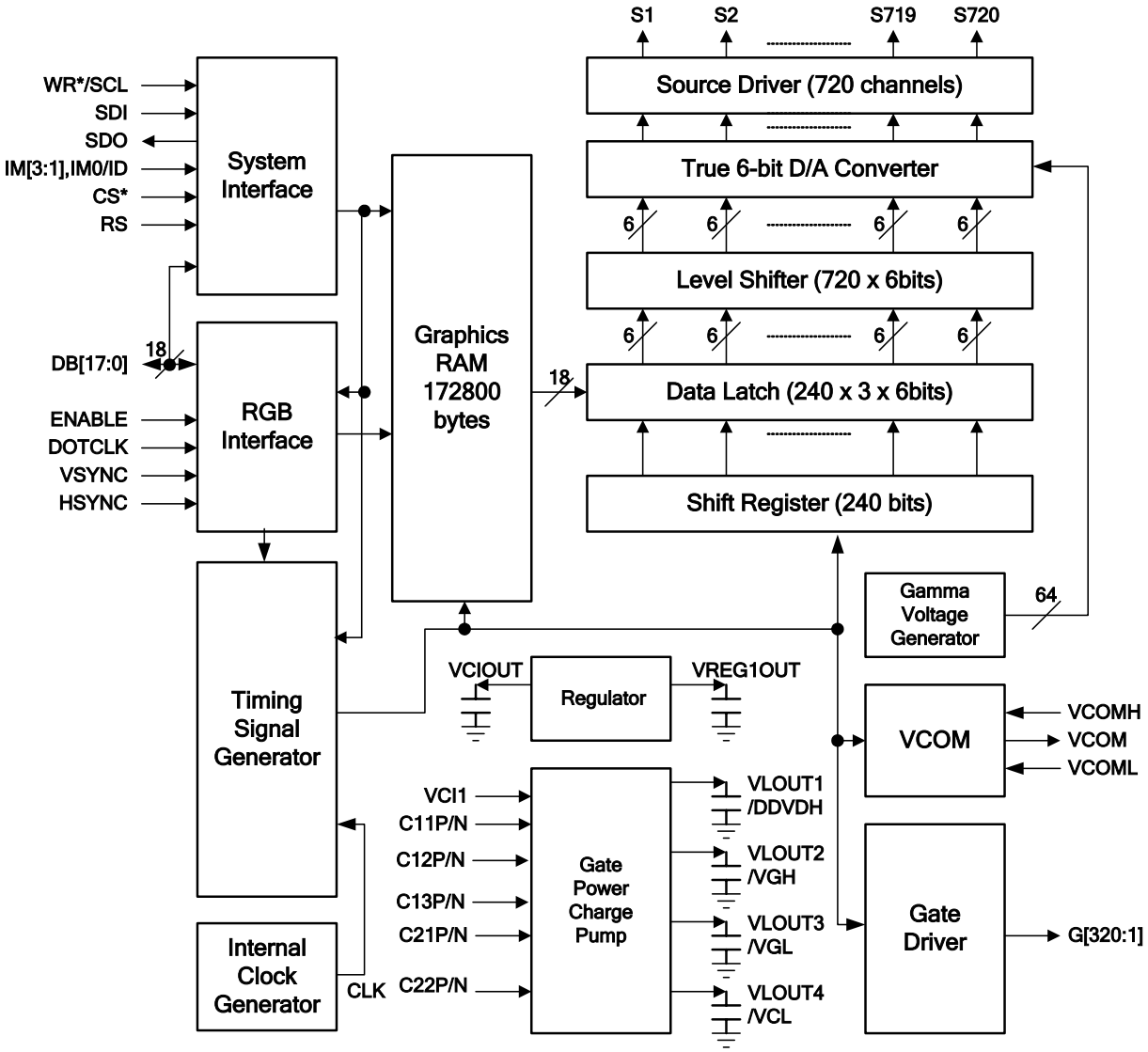
The built-in timing controller in OTM3225C can support several interfaces for the diverse request of medium or small size portable display. OTM3225C provides system interfaces, which include 8-/9-/16-/18-bit parallel interfaces and serial interface (SPI), to configure system. Not only can the system interfaces be used to configure system, they can also access RAM at high speed for still picture display. In addition, the OTM3225C incorporates 6, 8, 16, and 18-bit RGB interfaces for picture movement display. The OTM3225C also supports a function to display eight colors and a standby mode for power control consideration.

2. FEATURE

- One-chip solution for amorphous TFT-LCD.
- Supports resolution up to 240xRGBx320, incorporating a 720-channel source driver and a 320-channel gate driver
- Outputs 64 γ -corrected values using an internal true 6-bit resolution D/A converter to achieve 262K colors
- Built-in 172800 bytes internal RAM
- Line Inversion AC drive / frame inversion AC drive
- System interfaces
  - Intel 80-system with 8-, 9-, 16-, and 18-bit parallel ports
  - Serial Peripheral Interface (SPI)
- Interfaces for moving picture display
  - 6-, 8-, 16-, and 18-bit RGB interfaces
- Diverse RAM accessing for functional display
  - Window address function to display at any area on the screen via a moving picture display interface
  - Window address function to limit the data rewriting area and reduce data transfer
  - Moving and still picture can display at the same time
  - Vertical scrolling function
  - Partial screen display
- Power supply
  - I/O interface supply voltage (IOVCC): 1.65 ~ 3.3 V
  - Analog power supply voltage (VCI): 2.5 ~ 3.3 V
- Resize function(x 1/2, x 1/4)
- On-chip power management system
  - Power saving mode (standby / 8-color mode, etc)
  - Low power consumption structure for source driver.
- Built-in Charge Pump circuits
  - Source driver voltage level: DDVDH-GND=4.5V ~ 6V.
  - Gate driver voltage level (VGH, VGL)
    VGH = 10.0V ~20.0V
    VGL = -4.5V ~ -16.5V
    VGH – VGL < 30.0V
  - Built-in internal oscillator and hardware reset

3. BLOCK DIAGRAM

3.1. Block Function



3.2. System Interface

3.2.1. Interface

The OTM3225C supports two kinds of system interfaces:

Intel 80-system interfaces with 8-, 9-, 16-, 18-bits parallel port.

1. Serial Peripheral Interface (SPI).

The OTM3225C has a 16-bit index register (IR) and two 18-bit data registers; a write-data register (WDR) and a read-data register (RDR). The IR register is used to store index information from control registers. The WDR register is used to temporarily store data to be written for register control and internal GRAM. The RDR register is used to temporarily store data read from the GRAM or control register.

When graphic data is written to the internal GRAM from MCU's graphic engine, the data is first written to the WDR and then automatically written to the internal GRAM in internal operation. When graphic data read operation is executed, graphic data is read via the RDR from the internal GRAM. Therefore, invalid data is first read out to the data bus when the OTM3225C executes the 1st read operation. Thus, valid data can be read out after the OTM3225C executes the 2nd read operation.

3.2.2. External Display Interface

The OTM3225C supports external RGB interface for picture movement display.

The OTM3225C allows switching between one of the external display interfaces and the system interface via pin configuration so that the optimum interface is selected for still / moving picture displayed on the screen.

When the RGB interface is chosen, display operations are synchronized with external supplied signals, VSYNC, HSYNC, and DOTCLK. Moreover, valid display data (DB17-0) is written to GRAM, which synchronized with signal (ENABLE) enabling.

3.2.3. Address Counter (AC)

OTM3225C features an Address Counter (AC) giving an address to the internal GRAM. The address in the AC is automatically updated plus or minus 1. The window address function enables writing data only in the rectangular area arbitrarily set by users on the GRAM.

3.2.4. Graphics RAM (GRAM)

OTM3225C features a 172800-byte (240 x 320 x 18 / 8) Graphic RAM (GRAM).

3.2.5. Grayscale Voltage Generating Circuit

OTM3225C has true 6-bit resolution D/A converter, which generates 64 Gamma-corrected values and cooperates with OP-AMP structure to enhance display quality. The grayscale voltage can be adjusted by grayscale data set in the γ-correction register.

3.2.6. Timing Controller

OTM3225C has a timing controller, which can generate a timing signal for internal circuit operation such as gate output timing, RAM accessing timing, etc.

3.2.7. Oscillator (OSC)

The OTM3225C also features an internal oscillator to generate RC oscillation with an internal resistor. In standby mode, RC oscillation is halted to reduce power consumption.

3.2.8. Source Driver Circuit

OTM3225C consists of a 720-output source driver circuit (S1 ~ S720). Data in the GRAM are latched when the 720th bit data is input. The latched data controls the source driver and generates a drive waveform.

3.2.9. Gate Driver Circuit

OTM3225C consists of a 320-output gate driver circuit (G1~G320). The gate driver circuit outputs gate driver signals at either VGH or VGL level.

3.2.10. LCD Driving Power Supply Circuit

The LCD driving power supply circuit generates the voltage levels DDVDH, VGH, VGL and VCOM for driving an LCD. All this voltages can be adjusted by register setting.

4. SIGNAL DESCRIPTIONS

<table>
<tr><th>Signal</th><th>I/O</th><th>Connected with</th><th>Function</th></tr>
<tr><td colspan="4">System Configuration Input Signal</td></tr>
<tr><td>IM3~1, IM0/ID</td><td>I</td><td>GND/ IOVCC</td><td>Select an interface mode to MPU.
In serial interface operation, the IM0 pin is used to set the ID bit of device code.
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0/ I D</th><th>Interface Mode</th><th>DB Pin</th><th>Colors</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>80-system 16-bit interface</td><td>DB17-10, DB8-1</td><td>262,144 or 65,536</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>80-system 8-bit interface</td><td>DB17-10</td><td>262,144 or 65,536</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>*(ID)</td><td>Clock synchronous serial interface</td><td>-</td><td>262,144 or 65,536</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>80-system 18-bit interface</td><td>DB17-0</td><td>262,144 only</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>80-system 9-bit interface</td><td>DB17-9</td><td>262,144 only</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
</table></td></tr>
<tr><td>/RESET</td><td>I</td><td>MPU</td><td>RESET pin. This is an active low signal.</td></tr>
<tr><td colspan="4">Interface input Signals</td></tr>
<tr><td>/CS</td><td>I</td><td>MPU</td><td>Chip select signal.
Low: the OTM3225C is accessible.
High: the OTM3225C is not accessible.
Must connect to MPU.</td></tr>
<tr><td>RS</td><td>I</td><td>MPU</td><td>Register select signal.
Low: Index register or internal status is selected.
High: Control register is selected.
Must connect to the GND or IOVCC level when not used.</td></tr>
<tr><td>(/WR) / (SCL)</td><td>I</td><td>MPU</td><td>(A) In 80-system interface mode, a write strobe signal can be input via this pin and initializes a write operation when the signal is low.
(B) In SPI mode, served as a synchronizing clock signal.</td></tr>
<tr><td>/RD</td><td>I</td><td>MPU</td><td>In 80-system interface mode, a read strobe signal can be input via this pin and initializes a read operation when the signal is low.
Must connect to the GND or IOVCC level when not in use.</td></tr>
<tr><td>SDI</td><td>I</td><td>MPU</td><td>Serial Data is the input on the rising edge of the SCL signal in SPI mode.
Must connect to the GND or IOVCC level when not in use.</td></tr>
<tr><td>SDO</td><td>O</td><td>MPU</td><td>Serial Data is the output on the rising edge of the SCL signal in SPI mode.
Must keep this pin open (floating) when not used.
Can not connect to the GND or IOVCC level when not in use.</td></tr>
</table>

<table>
<tr><th>Signal</th><th>I/O</th><th>Connected with</th><th>Function</th></tr>
<tr><td>DB0-DB17</td><td>I/O</td><td>MPU</td><td>Served as an 18-bit parallel bi-directional data bus. Data bus pin assignment corresponding to different modes are summarized in the table:
<table>
<tr><th>Mode</th><th>Pin Assignment</th></tr>
<tr><td>8-bit system interface</td><td>DB17-DB10</td></tr>
<tr><td>9-bit system interface</td><td>DB17-DB9</td></tr>
<tr><td>16-bit system interface</td><td>DB17-DB10, DB8-DB1</td></tr>
<tr><td>18-bit system interface</td><td>DB17-DB0</td></tr>
<tr><td>6-bit External (RGB) interface</td><td>DB17-DB12</td></tr>
<tr><td>8-bit External (RGB) interface</td><td>DB17-DB10</td></tr>
<tr><td>16-bit External (RGB) interface</td><td>DB17-13, DB11-DB1</td></tr>
<tr><td>18-bit External (RGB) interface</td><td>DB17-DB0</td></tr>
<tr><td>Serial interface(SPI)</td><td>Not use</td></tr>
</table>
Must connect to the GND or IOVCC level when not in use.</td></tr>
<tr><td>VSYNC</td><td>I</td><td>MPU</td><td>In external RGB interface mode, served as a vertical synchronize signal input
Must connect to the IOVCC or GND level when not in use.</td></tr>
<tr><td>HSYNC</td><td>I</td><td>MPU</td><td>In external RGB interface mode, served as a horizontal synchronized signal input
Must connect to the IOVCC or GND level when not used.</td></tr>
<tr><td>ENABLE</td><td>I</td><td>MPU</td><td>In external RGB interface mode, polarity of ENABLE signal is synchronized with valid graphic data input.
Low: Valid data on DB17-DB0 (relative to different interface modes)
High: Invalid data on DB17-DB0 (relative to different interface modes)
Moreover, setting EPL bit can change the polarity of the ENABLE signal.
Must connect to the GND or IOVCC level when not in use.</td></tr>
<tr><td>DOTCLK</td><td>I</td><td>MPU</td><td>In external RGB interface mode, served as a dot clock signal.
When DPL = “0”: Input data on the rising edge of DOTCLK
When DPL = “1”: Input data on the falling edge of DOTCLK
It is fixed to the IOVCC or GND level when not in use.</td></tr>
<tr><td>FMARK</td><td>O</td><td>MPU</td><td>Frame head pulse signal, which is used when writing data to the internal RAM.
Must keep this pin open(floating) when not used.
Can not connect to the GND or IOVCC level when not in use.</td></tr>
<tr><td colspan="4">Charge Pump and Power Supply Signal</td></tr>
<tr><td>C11P/N,
C12P/N
C13P/N
C21P/N,
C22P/N</td><td>-</td><td>Step-up capacitor</td><td>Connect boost capacitors for the internal DC/DC converter circuit to these pins.</td></tr>
<tr><td>VCI1</td><td>I/O</td><td>Stabilizing capacitor</td><td>Reference voltage of step-up circuit 1. Make sure the output voltage levels from DDVDH, VGH, and VGL do not exceed the respective setting ranges.</td></tr>
<tr><td>DDVDH</td><td>I</td><td>Stabilizing capacitor</td><td>Power supply for the source driver liquid crystal drive unit and VCOM drive. DDVDH = 4.5V ~ 6.0V</td></tr>
<tr><td>VGH</td><td>I</td><td>Stabilizing capacitor</td><td>Liquid crystal driving power supply.</td></tr>
<tr><td>VGL</td><td>I</td><td>Stabilizing capacitor</td><td>Liquid crystal driving power supply.</td></tr>
<tr><td>VCL</td><td>O</td><td>Stabilizing capacitor</td><td>VCOML drive power supply. Make sure to connect to stabilizing capacitor. VCL = -1.9V ~ -3.0V</td></tr>
</table>

Signal	I/O	Connected with	Function
LEDPWM/ TESTO1	O	LED Driver	Output PWM signal, which control LED driver for backlight dimming. Must connect to the GND level or Open (floating) when not in use.
LEDON/ TESTO2	O	LED Driver	Output control signal for turn ON/OFF LED backlight. Must connect to the GND level or Open (floating) when not in use.
Source/Gate Driver and VCOM Signals			
G1~G320	O	LCD	Output gate driver signals, which has the swing from VGH to VGL
S1~S720	O	LCD	Output source driver signals. The D/A converted 64-gray-scale analog voltage are output.
VREG1OUT	O	Stabilizing capacitor	Output voltage generated from the reference voltage (VCI or VCIR). The factor is determined by instruction (VRH bits). VREG1OUT is used for : (1) Source driver grayscale reference voltage (2) VCOMH level reference voltage (3) VCOM amplitude reference voltage Connect to a stabilizing capacitor when in use. VREG1OUT = 4.0V ~ (DDVDH – 0.5)V
VCOM	O	TFT panel common electrode	Power supply to TFT panel's common electrode. VCOM alternates between VCOMH and VCOML. The alternating cycle is set by internal register. Also, the VCOM output can be started and halted by register setting.
VCOMH	O	Stabilizing capacitor	The High level of VCOM amplitude. The output level can be adjusted by electronic volume. Make sure to connect to stabilizing capacitor.
VCOML	O	Stabilizing capacitor	The Low level of VCOM amplitude. The output level can be adjusted by instruction (VDV bits). VCOML = (VCL+0.5) V ~ 0V. Make sure to connect to stabilizing capacitor.
VGS	I	GND	Reference level for the grayscale voltage generating circuit. Must connect to the GND level for normal usage.
GND	P	Power supply	Internal logic GND: GND = 0V.
RGND	P	Power supply	Internal RAM GND. RGND must be at the same electrical potential as GND. In case of COG, connect to GND on the FPC to prevent noise.
VDDD	O	Stabilizing capacitor	Internal logic regulator output, which is used as the power supply to internal logic. Connect to stabilizing capacitor.
IOVCC	P	Power supply	Power supply to the interface pins: /RESET, /CS, /WR, /RD, RS, DB17-0, VSYNC, HSYNC, DOTCLK, ENABLE. IOVCC = 1.65V ~ 3.3V. Note: Must keep VCI ≥IOVCC.
AGND	P	Power supply	Analog GND (for logic regulator and liquid crystal power supply circuit): AGND = 0V. In case of COG, connect to GND on the FPC to prevent noise.
VCI	P	Power supply	Power supply to the liquid crystal power supply analog circuit. Connect to an external power supply of 2.5V ~ 3.3V.
Misc. Signal			
IOGNDDUM	I/O	Open	Test pins. Leave them open.
DUMMY1~15 DUMMY20~27	I/O	Open	Test pins. Leave them open.
TESTO3~16	I/O	Open	Test pins. Leave them open.
TEST1~3	I/O	Open	Test pins. Leave them open.
TS0~8	I/O	Open	Test pins. Leave them open

5. INSTRUCTIONS

5.1. Outline

The OTM3225C supports 18-bit data bus interface to access command register to configure system. When the command register accessing is desired, sending the command information to specify which index register would be accessed and following the data to that control register. Moreover, register accessing operation should cooperate with RS, /WR, /RD signal for OTM3225C to recognize the control instruction. And command instruction can be accomplished by using all system interfaces (18-bit, 16-bit, 9-bit, 8-bit 80-system and SPI). The corresponding pin assignment of different system interface are shown in Figure 5-1 to Figure 5-5

The instruction can be categorized into 9 groups. And the 9 groups are:

1. Specify the index of register
2. Read a status
3. Display control
4. Power management Control
5. Graphics data processing
6. Set internal GRAM address
7. Transfer data to and from the internal GRAM
8. Internal grayscale γ-correction
9. CABC Function (CABC= Content Adaptive Brightness Control)

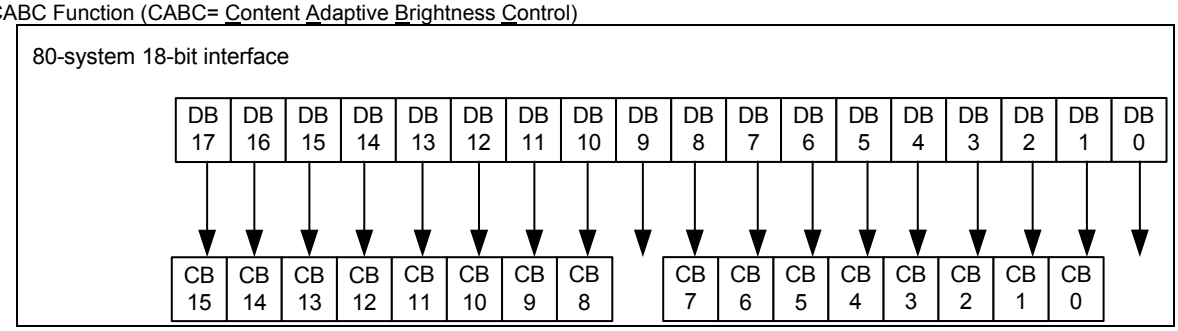


Figure 5-1 : I80-system 18bits interface data transfer format

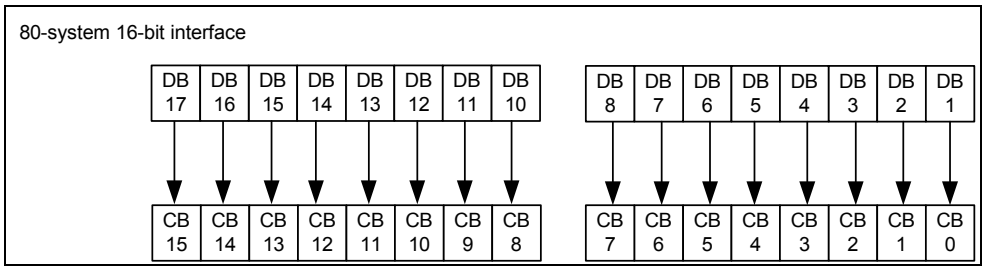


Figure 5-2 : I80-system 16bits interface data transfer format

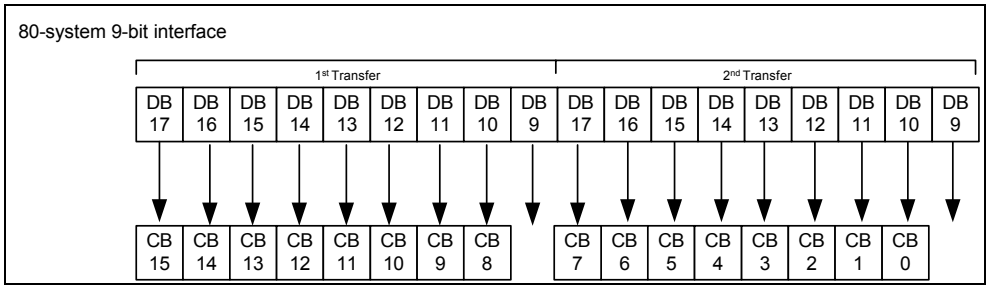


Figure 5-3 : I80-system 9bits interface data transfer format

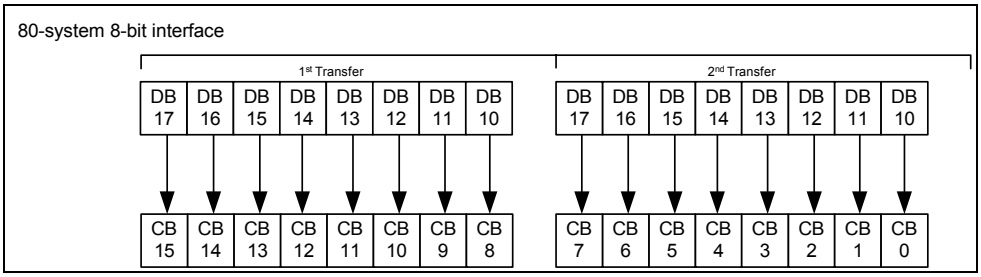


Figure 5-4 : I80 8bits interface data transfer format

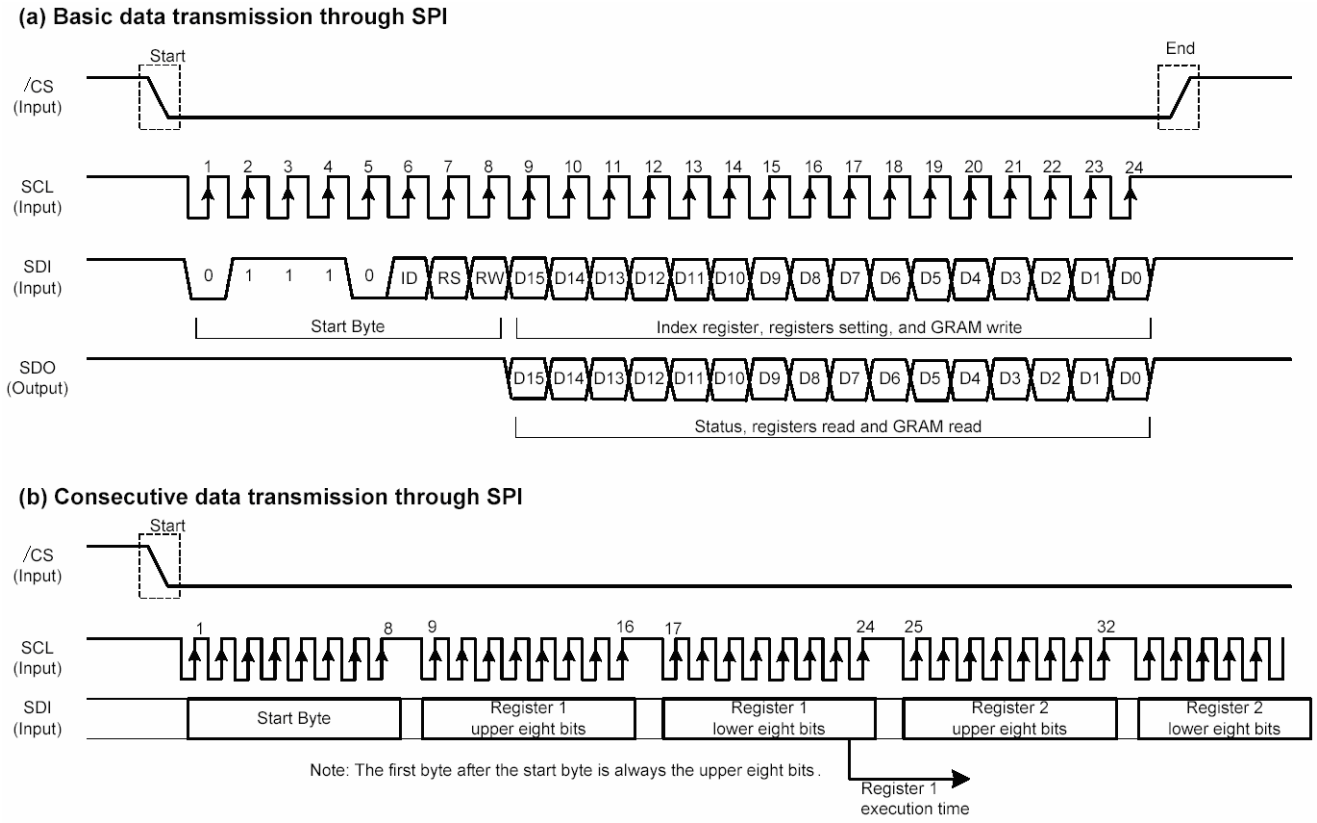


Figure 5-5 : Serial interface data transfer format

5.2. Instruction

Table 5-1 Instruction List Table

Register No	Register	Upper 8-bit								Lower 8-bit							
		CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
00h	ID Read	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0
01h	Driver Output Control	0	0	0	0	0	SM (0)	0	SS (0)	0	0	0	0	0	0	0	0
02h	LCD Drive Waveform Control	0	0	0	0	0	1	B/C (0)	EOR (0)	0	0	0	0	0	0	0	0
03h	Entry Mode	TRI (0)	DFM (0)	0	BGR (0)	0	0	0	0	ORG (0)	0	I/D1 (1)	I/D0 (1)	AM (0)	0	0	0
04h	Scaling Control	0	0	0	0	0	0	RCV1 (0)	RCV0 (0)	0	0	RCH1 (0)	RCH0 (0)	0	0	RSZ1 (0)	RSZ0 (0)
07h	Display Control (1)	0	0	PTDE1 (0)	PTDE0 (0)	0	0	0	BASEE (0)	0	0	GON (0)	DTE (0)	CL (0)	0	D1 (0)	D0 (0)
08h	Display Control (2)	0	0	0	0	FP3 (1)	FP2 (0)	FP1 (0)	FP0 (0)	0	0	0	0	BP3 (1)	BP2 (0)	BP1 (0)	BP0 (0)
09h	Display Control (3)	0	0	0	0	0	PTS2 (0)	PTS1 (0)	PTS0 (0)	0	0	PTG1 (0)	PTG0 (0)	ISC3 (0)	ISC2 (0)	ISC1 (0)	ISC0 (0)
0Ah	Frame Cycle Control	0	0	0	0	0	0	0	0	0	0	0	0	FMARKOE (0)	FMI2 (0)	FMI1 (0)	FMI0 (0)
0Ch	External Display interface control (1)	0	ENC2 (0)	ENC1 (0)	ENC0 (0)	0	0	0	RM (0)	0	0	DM1 (0)	DM0 (0)	0	0	RIM1 (0)	RIM0 (0)
0Dh	Frame Maker Position	0	0	0	0	0	0	0	FMP8 (0)	FMP7 (0)	FMP6 (0)	FMP5 (0)	FMP4 (0)	FMP3 (0)	FMP2 (0)	FMP1 (0)	FMP0 (0)
0Fh	External Display interface control (2)	0	0	0	0	0	0	0	0	0	0	0	VSPL (0)	HSPL (0)	0	EPL (0)	DPL (0)
10h	Power Control (1)	0	0	0	SAP (0)	0	BT2 (0)	BT1 (0)	BT0 (0)	APE (0)	AP2 (1)	AP1 (0)	AP0 (0)	0	0 (1)	SLP (0)	STB (0)
11h	Power Control (2)	0	0	0	0	0	DC12 (1)	DC11 (1)	DC10 (1)	0	DC02 (1)	DC01 (1)	DC00 (1)	0	VC2 (0)	VC1 (0)	VC0 (0)
12h	Power Control (3)	0	0	0	0	0	0	0	0	VCIRE (0)	0	0	1	VRH3 (0)	VRH2 (0)	VRH1 (0)	VRH0 (0)
13h	Power Control (4)	0	0	0	VDV4 (0)	VDV3 (0)	VDV2 (0)	VDV1 (0)	VDV0 (0)	0	0	0	0	0	0	0	0
20h	GRAM address Set Horizontal Address	0	0	0	0	0	0	0	0	AD7 (0)	AD6 (0)	AD5 (0)	AD4 (0)	AD3 (0)	AD2 (0)	AD1 (0)	AD0 (0)
21h	GRAM address Set Vertical Address	0	0	0	0	0	0	0	AD16 (0)	AD15 (0)	AD14 (0)	AD13 (0)	AD12 (0)	AD11 (0)	AD10 (0)	AD9 (0)	AD8 (0)
22h	Write Data to GRAM Read Data from GRAM																
29h	Power Control (7)	0	0	0	0	0	0	0	0	0	0	0	VCM4 (0)	VCM3 (0)	VCM2 (0)	VCM1 (0)	VCM0 (0)
2Bh	Frame Rate Control	0	0	0	0	0	0	0	0	0	0	0	0	FRS3 (1)	FRS2 (0)	FRS1 (1)	FRS0 (1)
30h	γ Control (1)	0	0	0	0	0	KP1[2] (0)	KP1[1] (0)	KP1[0] (0)	0	0	0	0	0	KP0[2] (1)	KP0[1] (0)	KP0[0] (0)
31h	γ Control (2)	0	0	0	0	0	KP3[2] (0)	KP3[1] (1)	KP3[0] (1)	0	0	0	0	0	KP2[2] (1)	KP2[1] (1)	KP2[0] (0)
32h	γ Control (3)	0	0	0	0	0	KP5[2] (0)	KP5[1] (0)	KP5[0] (0)	0	0	0	0	0	KP4[2] (0)	KP4[1] (1)	KP4[0] (1)
35h	γ Control (4)	0	0	0	0	0	RP1[2] (0)	RP1[2] (1)	RP1[0] (1)	0	0	0	0	0	RP0[2] (0)	RP0[2] (1)	RP0[0] (1)
36h	γ Control (5)	0	0	0	VRP1[4] (0)	VRP1[3] (1)	VRP1[2 (1)]	VRP1[1] (1)	VRP1[0] (0)	0	0	0	VRP0[4] (0)	VRP0[3] (0)	VRP0[2] (1)	VRP0[1] (1)	VRP0[0] (0)
37h	γ Control (6)	0	0	0	0	0	KN1[2] (1)	KN1[1] (0)	KN1[0] (0)	0	0	0	0	0	KN0[2] (1)	KN0[1] (1)	KN0[0] (1)
38h	γ Control (7)	0	0	0	0	0	KN3[2] (0)	KN3[1] (0)	KN3[0] (1)	0	0	0	0	0	KN2[2] (1)	KN2[1] (0)	KN2[0] (0)
39h	γ Control (8)	0	0	0	0	0	KN5[2] (0)	KN5[1] (1)	KN5[0] (1)	0	0	0	0	0	KN4[2] (1)	KN4[1] (1)	KN4[0] (1)
3Ch	γ Control (9)	0	0	0	0	0	RN1[2] (0)	RN1[1] (1)	RN1[0] (1)	0	0	0	0	0	RN0[2] (0)	RN0[1] (1)	RN0[0] (10)
3Dh	γ Control (10)	0	0	0	VRN1[4] (0)	VRN1[3] (0)	VRN1[2] (1)	VRN1[1] (0)	VRN1[0] (0)	0	0	0	VRN0[4] (0)	VRN0[3] (1)	VRN0[2] (0)	VRN0[1] (1)	VRN0[0] (1)
50h	Window Horizontal RAM Address Start	0	0	0	0	0	0	0	0	HSA7 (0)	HSA6 (0)	HSA5 (0)	HSA4 (0)	HSA3 (0)	HSA2 (0)	HSA1 (0)	HSA0 (0)
51h	Window Horizontal RAM Address End	0	0	0	0	0	0	0	0	HEA7 (1)	HEA6 (1)	HEA5 (1)	HEA4 (0)	HEA3 (1)	HEA2 (1)	HEA1 (1)	HEA0 (1)
52h	Window Vertical RAM Address Start	0	0	0	0	0	0	0	VSA8 (0)	VSA7 (0)	VSA6 (0)	VSA5 (0)	VSA4 (0)	VSA3 (0)	VSA2 (0)	VSA1 (0)	VSA0 (0)
53h	Window Vertical RAM Address End	0	0	0	0	0	0	0	VEA8 (1)	VEA7 (0)	VEA6 (0)	VEA5 (1)	VEA4 (1)	VEA3 (1)	VEA2 (1)	VEA1 (1)	VEA0 (1)
60h	Driver Output Control	GS (0)	0	NL5 (1)	NL4 (0)	NL3 (0)	NL2 (1)	NL1 (1)	NL0 (1)	0	0	SCN5 (0)	SCN4 (0)	SCN3 (0)	SCN2 (0)	SCN1 (0)	SCN0 (0)
61h	Driver Output Control	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL (0)	VLE (0)	REV (0)
6Ah	Vertical Scroll Control	0	0	0	0	0	0	0	VL8 (0)	VL7 (0)	VL6 (0)	VL5 (0)	VL4 (0)	VL3 (0)	VL2 (0)	VL1 (0)	VL0 (0)
80h	Display Position - Partial Display 1	0	0	0	0	0	0	0	PTDP08 (0)	PTDP07 (0)	PTDP06 (0)	PTDP05 (0)	PTDP04 (0)	PTDP03 (0)	PTDP02 (0)	PTDP01 (0)	PTDP00 (0)
81h	RAM Address Start - Partial Display 1	0	0	0	0	0	0	0	PTSA08 (0)	PTSA07 (0)	PTSA06 (0)	PTSA05 (0)	PTSA04 (0)	PTSA03 (0)	PTSA02 (0)	PTSA01 (0)	PTSA00 (0)
82h	RAM Address End - Partial Display 1	0	0	0	0	0	0	0	PTEA08 (0)	PTEA07 (0)	PTEA06 (0)	PTEA05 (0)	PTEA04 (0)	PTEA03 (0)	PTEA02 (0)	PTEA01 (0)	PTEA00 (0)
83h	Display Position - Partial Display 2	0	0	0	0	0	0	0	PTDP18 (0)	PTDP17 (0)	PTDP16 (0)	PTDP15 (0)	PTDP14 (0)	PTDP13 (0)	PTDP12 (0)	PTDP11 (0)	PTDP10 (0)

Register No	Register	Upper 8-bit								Lower 8-bit							
		CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
84h	RAM Address Start - Partial Display 2	0	0	0	0	0	0	0	PTSA18 (0)	PTSA17 (0)	PTSA16 (0)	PTSA15 (0)	PTSA14 (0)	PTSA13 (0)	PTSA12 (0)	PTSA11 (0)	PTSA10 (0)
85h	RAM Address End - Partial Display 2	0	0	0	0	0	0	0	PTEA18 (0)	PTEA17 (0)	PTEA16 (0)	PTEA15 (0)	PTEA14 (0)	PTEA13 (0)	PTEA12 (0)	PTEA11 (0)	PTEA10 (0)
90h	Panel interface Control 1	0	0	0	0	0	0	DIVI1 (0)	DIVI0 (0)	0	0	0	RTNI4 (1)	RTNI3 (0)	RTNI2 (0)	RTNI1 (0)	RTNI0 (0)
92h	Panel Interface Control 2	0	0	0	0	0	NOWI2 (1)	NOWI1 (1)	NOWI0 (0)	0	0	0	0	0	0	0	0
95h	Panel Interface Control 4	0	0	0	0	0	0	DIVE1 (1)	DIVE0 (0)	0	0	RTNE5 (0)	RTNE4 (1)	RTNE3 (1)	RTNE2 (1)	RTNE1 (0)	RTNE0 (0)
97h	Panel Interface Control 5	0	0	0	0	NOWE3 (1)	NOWE2 (1)	NOWE1 (0)	NOWE0 (0)	0	0	0	0	0	0	0	0
B1h	Write Display Brightness Value	0	0	0	0	0	0	0	0	DBV7 (0)	DBV6 (0)	DBV5 (0)	DBV4 (0)	DBV3 (0)	DBV2 (0)	DBV1 (0)	DBV0 (0)
B2h	Read Display Brightness Value	0	0	0	0	0	0	0	0	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0
B3h	Write Control Display Value	0	0	0	0	0	0	LED_ON (0)	BC_OUT_INV (0)	0	0	BCTRL (0)	0	DD (0)	BL (0)	0	0
B4h	Read Control Display Value	0	0	0	0	0	0	LED_ON	BC_OUT_INV			BCTRL		DD	BL		
B5h	Write Content Adaptive Brightness Control Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C1 (0)	C0 (0)
B6h	Read Content Adaptive Brightness Control Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C1	C0
BEh	Write CABC minimum brightness	0	0	0	0	0	0	0	0	CMB7 (0)	CMB6 (0)	CMB5 (0)	CMB4 (0)	CMB3 (0)	CMB2 (0)	CMB1 (0)	CMB0 (0)
BFh	Read CABC minimum brightness	0	0	0	0	0	0	0	0	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0

The following are detailed explanations of instructions with illustrations of instruction bits (CB15-0) assigned to each interface.

5.2.1. Index Register (IR)

R/W	RS	CB15	CCB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	0	*	*	*	*	*	*	*	*	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

The index register specifies the index (R00h ~ RFFh) of a control register or RAM. The index range is from “0000_0000” to “1111_1111” in binary format.

5.2.2. Read ID Register

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
R	1	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

The IC code of OTM3225C can be accessed by read operation. The 16-bits ID Code can be read out when read ID operation is executed. The ID information can be set from 0x0000h to 0xFFFFh by IC metal option or Trim option for customer’s request.

5.2.3. Driver Output Control Register (R01h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0

SS: Shift direction of the source driver output selection.

When SS = “0”, source driver shift from S1 to S720.

When SS =“1”, source driver shift from S720 to S1. Moreover, SS can cooperate with BGR for different color filter configuration of LCD panel. The combination of SS and BGR bit are summarized at **Table 5-2**.

★**Note:** After changing SS bit or BGR bit, display data must be rewritten.

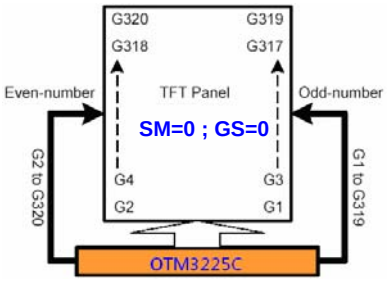
Table 5-2

SS=0;BGR=0;	S1	S2	S3	→	S718	S719	S720
SS=0;BGR=1;	S1	S2	S3	→	S718	S719	S720
SS=1,BGR=0;	S1	S2	S3	←	S718	S719	S720
SS=1,BGR=1;	S1	S2	S3	←	S718	S719	S720

SM: Set the scan mode of the gate driver output. Moreover, SM can cooperate with GS for different LCD panel gate line layout. The combination of GS and SM bit are summarized at **Table 5-3** and **Figure 5-6**

Table 5-3

SM	GS	Gate output sequence (Begin,…..,End)
0	0	G1→G2→G3→G4→….→G317→G318→G319→G320
0	1	G320→G319→G318→G317→,…→G4→G3→G2→G1
1	0	G1→G3→G5→,…→G317→G319→ →G2→G4→G6→,...→G318→G320
1	1	G32()→G318→G316→….→G4→G2→ →G319→G317→G315→....→G3→G1



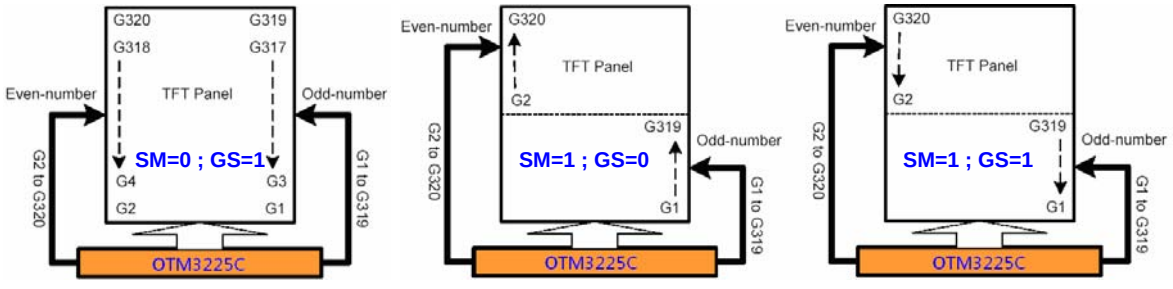


Figure 5-6{ TC }: Panel layout for SM & GS bit

5.2.4. LCD Driving Waveform Control (R02h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	1	BC0	EOR	0	0	0	0	0	0	0	0

BC0: This bit can set the VCOM toggle at ever frame format or N-line inversion format.

BC0=0: Frame inversion waveform is selected.

BC0=1: Line inversion waveform is selected. (Must combine EOR=1 for Line inversion)

EOR: Enables Line-inversion when EOR=1 and BC0=1.

5.2.5. Entry Mode (R03h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	TRI	DFM	0	BGR	0	0	0	0	ORG	0	I/D1	I/D0	AM	0	0	0

Table 5-4

Operation mode	ORG	AM	I/D1	I/D0	Function
Mode 1	0	0	0	0	Replace horizontal data
Mode2	0	1	0	1	Replace vertical data
Mode3	1	0	1	0	Conditionally replace horizontal data
Mode4	1	1	1	1	Conditionally replace vertical data

★**Note:** After changing ORG;AM;I/D1 or I/D0 bit, display data must be rewritten.

AM: To set the update direction when writing data to GRAM.

If AM=1, data will write in vertical direction. (Address counter will automatic update in vertical direction)

If AM=0, data will write in horizontal direction. (Address counter will automatic update in horizontal direction)

When setting a window area by register R50h~R53h, the data is written only within the area based on by I/D[1:0],AM bit.

I/D1-0: To specify address counter(AC) automatically increment or decrement while update one pixel display data to GRAM.

I/D[0] indicates the increment or decrement in horizontal direction.

I/D[0]=0: decrement in horizontal direction automatically

I/D[0]=1: increment in horizontal direction automatically

I/D[1] indicates the increment or decrement in vertical direction.

I/D[1]=0: decrement in vertical direction automatically

I/D[1]=1: increment in vertical direction automatically

ID[1-0] setting can cooperate with AM bit to set the data updating direction.

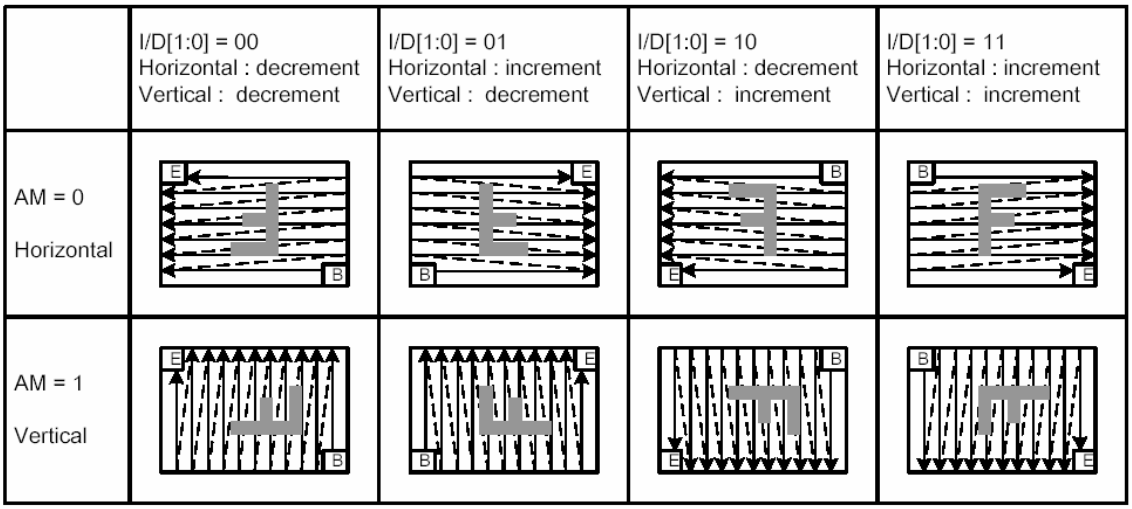


Figure 5-7

ORG: OTM3225C provides the option of start address definition when window function is selected.

ORG=0: RAM address setting (R20h, R21h) should set to the window start address, as normal operation case.

In this case, the origin address is not move.

ORG=1: RAM address setting (R20h, R21h) should set to (0x0000h) no matter where the window start address is.

Setting other addresses is inhibited.

In this case, the window start position is treated as (0x0000h), regardless the physical location in GRAM.

★**Note:** In GRAM read operation(R22h), make sure to set ORG=0.

★**Note:** In RGB mode with Full-Screen operation, make sure to set ORG=1.

BGR: To set the order of RGB sub-pixel in GRAM.

The combination of SS and BGR bit are summarized at **Table 5-2**.

BGR=0: same assignment of RGB allocation of DB17-0.

DB17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

BGR=1: inverse assignment of RGB allocation of DB17-0.

DB17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
B5	B4	B3	B2	B1	B0	G5	G4	G3	G2	G1	G0	R5	R4	R3	R2	R1	R0

Figure 5-8

DFM: In combination with TRI setting, sets the format to develop 16-/8-bit data to 18-bit data when using either 16-bit or 8-bit bus interface. Make sure to set DFM=0 when not transferring data via 16-bit or 8-bit interface.

TRI: to set 1–3 time transfer mode for system interface. TRI bit should cooperate with DFM to meet the specific transfer mode.

For 8-bit data bus interface mode:

TRI=0: 2 time transfer mode for 16-bit GRAM data.

TRI=1: 3 time transfer mode for 18-bit GRAM data

For 16-bit data bus interface mode:

TRI=0: 1 time transfer mode for 16-bit GRAM data.

TRI=1: 2 time transfer mode for 18-bit GRAM data

★**Note:** Set TRI=0, when using 18-bits bus width or 9-bits bus width.

★**Note:** The combination of DFM and TRI bit are summarized at **Figure 5-9 & 5-10**.

★**Note:** Must set TRI=0, when reading back data from GRAM. (Hint: Read GRAM data will be 16-bits only)

★**Note:** Set TRI=0, when using 65536 color format.

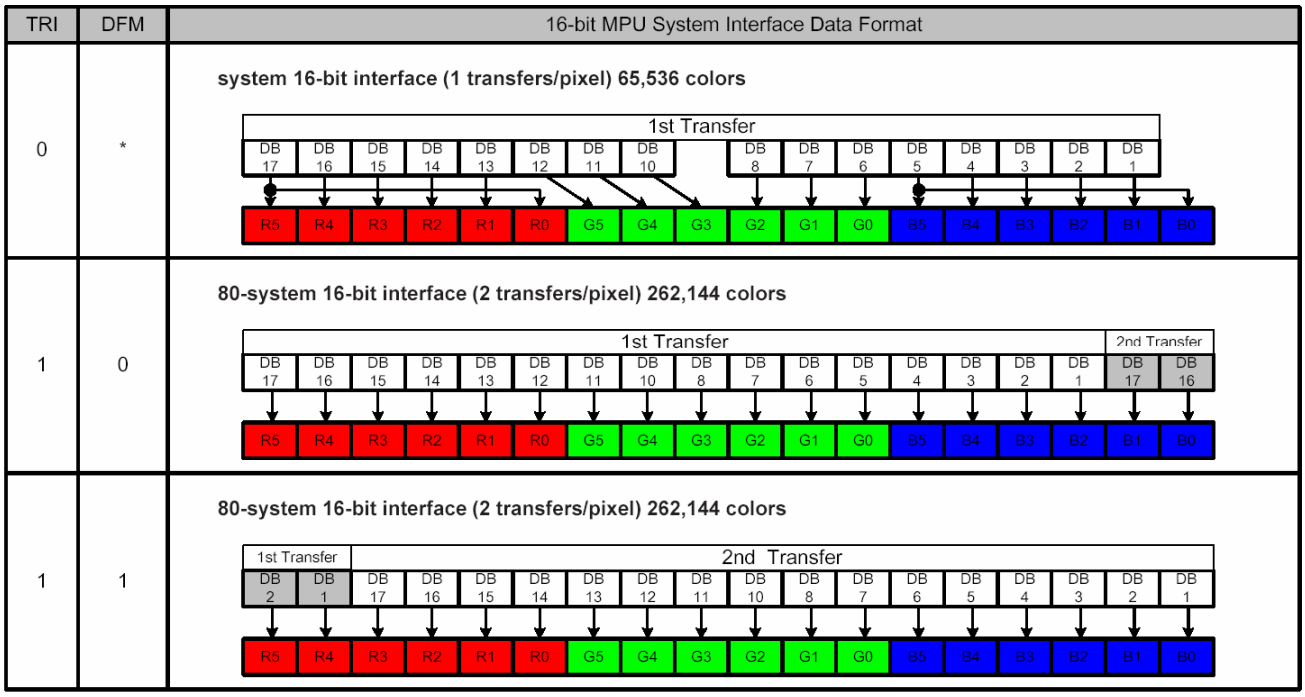


Figure 5-9

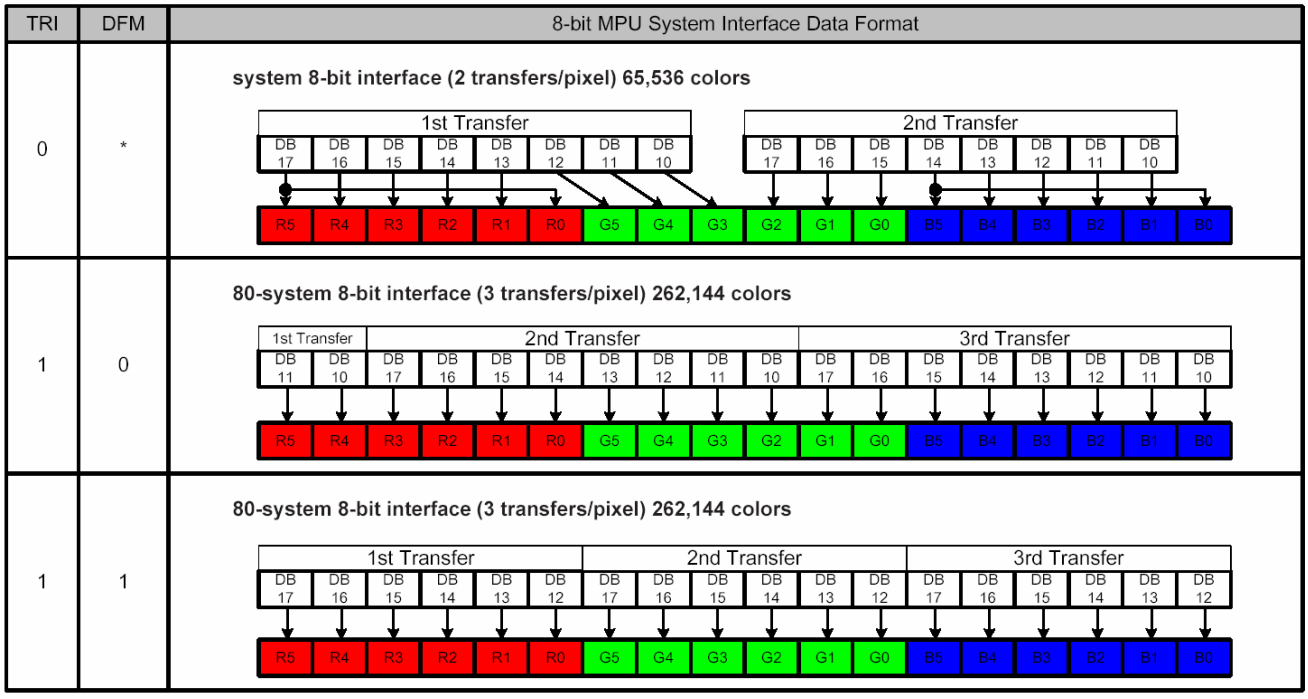


Figure 5-10

5.2.6. Scaling Control register (R04h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	RCV1	RCV0	0	0	RCH1	RCH0	0	0	RSZ1	RSZ0

RSZ [1:0]: OTM3225C provides scaling factor to give the display more flexibility to show different picture size. For detail, refer to “Scaling function”.

RSZ1	RSZ0	Scaling Factor
0	0	No Scaling
0	1	1/2 times
1	0	No Scaling
1	1	1/4 times

No Scaling 1/2 times 1/4 times

RCH [1:0]: To set the surplus pixel number in horizontal direction when scaling mode is selected. When scaling mode is not selected, make sure RCH [1:0]= “00”

RCH1	RCH0	Surplus pixel number in Horizontal direction
0	0	0 Pixel
0	1	1 Pixel
1	0	2 Pixels
1	1	3 Pixels

RCV [1:0]: To set the surplus pixel number in Vertical direction when scaling mode is selected. When scaling mode is not selected, make sure RCV [1:0]= “00”

RCV1	RCV0	Surplus pixel number in Vertical direction
0	0	0 Pixel
0	1	1 Pixel
1	0	2 Pixels
1	1	3 Pixels

5.2.7. Display Control (R07h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	PTDE1	PTDE0	0	0	0	BASEE	0	0	GON	DTE	COL	0	D1	D0

D1-0: To set the internal operation, source driver output and VCOM output function. When D1-0=00; OTM3225C is set to standby mode.

COL: 8-color mode selection. When COL=1 OTM3225C enter to 8-color mode. When COL=0, OTM3225C is in normal operation mode.

The combination of D1-0 , COL and BASEE bit is summarized at 錯誤! 書籤的自我參照不正確。.

Table 5-5

D1-0	BASEE	COL	Source output	VCOM output	Internal Operation	Display Mode
00	*	*	GND	GND	Halt (Standby)	OFF
01	*	*	GND	GND	Halt (Standby)	OFF
10	*	*	V0 & V63 (Full)	Toggle	Normal Operation	8 Color
11	0	0	Non-lit display & Partial	Toggle	Normal Operation	Partial
	0	1	Non-lit display & Partial	Toggle	Normal Operation	Partial + 8 Color
	1	0	Normal display (Full)	Toggle	Normal Operation	Normal
	1	1	V0 & V63 (Full)	Toggle	Normal Operation	8 Color

DTE: Specify the high/low level of gate driver output signal. The meaning of DTE bit is summarized at **Table 5-6**

Table 5-6

APE	DTE	Gate Output
1	0	VGL
	1	VGH/VGL

BASEE: To enable Base image display

BASEE	Display
0	(1) Non-lit display (2) Partial image display
1	Base image is display on the LCD

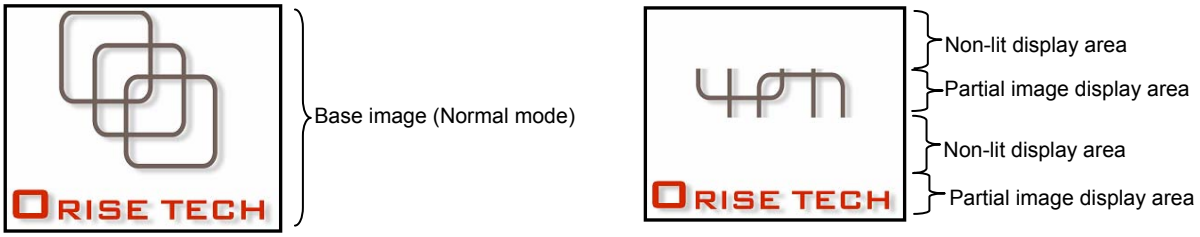
PTDE1-0: To set the partial-display enables function.

PTDE [0]: “0” Partial image 1 display “Off”.

“1” Partial image 1 display “On”.

PTDE [1]: “0” Partial image 2 display “Off”.

“1” Partial image 2 display “On”.



For detail information, refer to section “Partial Display function:”

5.2.8. Display Control 2 (R08h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0

FP3-0: Set the amount of blank period of front porch

BP3-0: Set the amount of blank period of back porch

Table 5-7 summarized the function of FP3-0/BP3-0 setting.

When setting this register, we recommend that:

BP + FP ≤ 16 lines

FP ≥ 2 lines

BP ≥ 2 lines

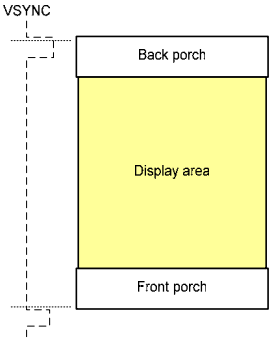


Figure 5-11 Front porch and back porch function diagram

In external display interface mode, a back porch (BP) period starts on the falling edge of the VSYNC signal, followed by a display operation period. After driving the number of lines set with NL bits, a front porch period starts. After the front porch period, a blank period continues until the next input of VSYNC signal. Be aware that different interface mode, has different BP/ FP setting. **Table 5-8** summarized the setting for each interface mode.

Table 5-7

FP3	FP2	FP1	FP0	Number of lines for the Front Porch
BP3	**BP2**	**BP1**	**BP0**	**Number of lines for the Back Porch**
0	0	0	0	1 lines
0	0	0	1	1 lines
0	0	1	0	2 lines
0	0	1	1	3 lines
0	1	0	0	4 lines
0	1	0	1	5 lines
0	1	1	0	6 lines
0	1	1	1	7 lines
1	0	0	0	8 lines
1	0	0	1	9 lines
1	0	1	0	10 lines
1	0	1	1	11 lines
1	1	0	0	12 lines
1	1	0	1	13 lines
1	1	1	0	14 lines
1	1	1	1	15 lines

Table 5-8 Recommend setting for BP & FP

Operation of Internal clock	BP ≥ 2 lines	FP ≥ 2 lines	FP +BP ≤ 16 lines
RGB interface	BP ≥ 2 lines	FP ≥ 2 lines	FP +BP ≤ 16 lines
VSYNC interface	BP ≥ 2 lines	FP ≥ 2 lines	FP +BP = 16 lines

5.2.9. Display Control 3 (R09h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	PTS2	PTS1	PTS0	0	0	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0

ISC3-0: To set the gate driver scan cycle in non-lit display area.

Table 5-9 summarized the function of ISC3-0 setting

Table 5-9

ISC3	ISC2	ISC1	ISC0	Scan cycle	fFLM=60Hz
0	0	0	0	1 Frames	16ms
0	0	0	1	1 Frames	16ms
0	0	1	0	3 Frames	50 ms
0	0	1	1	5 Frames	84 ms
0	1	0	0	7 Frames	117 ms
0	1	0	1	9 Frames	150 ms
0	1	1	0	11 Frames	184 ms
0	1	1	1	13 Frames	217 ms
1	0	0	0	15 Frames	251 ms
1	0	0	1	17 Frames	317 ms
1	0	1	0	19 Frames	351 ms
1	0	1	1	21 Frames	384 ms
1	1	0	0	23 Frames	418 ms
1	1	0	1	25 Frames	451 ms
1	1	1	0	27 Frames	484 ms
1	1	1	1	29 Frames	518 ms

PTG1-0: To set the gate driver scan mode in non-display area.

Table 5-10 summarized the function of PTG1-0 setting

Table 5-10

PTG1	PTG0	Gate outputs in non-display area	Source outputs in non-display area	VCOM output
0	0	Normal scan	Based on the PTS2-0 bits setting	VCOMH/VCOML
0	1	Normal scan	Based on the PTS2-0 bits setting	VCOMH/VCOML
1	0	Interval scan	Based on the PTS2-0 bits setting	VCOMH/VCOML
1	1	Normal scan	Based on the PTS2-0 bits setting	VCOMH/VCOML

PTS2-0: To set the source driver output level in non-display area of partial display mode. **Table 5-11** summarized the function of PTS2-0 setting.

Table 5-11

PTS2	PTS1	PTS0	Source output in non-display area		Operation amplifier in non-display area	Display in non-display area (Normally White panel)
			+ polarity	- polarity		
0	0	0	V63	V0	V0~V63	White
0	0	1	V0	V63	V0~V63	Black
0	1	0	GND	GND	V0~V63	White (With Flicker)
0	1	1	High impedance	High impedance	V0~V63	Abnormal (Crosstalk)
1	0	0	V63	V0	V0~V63	White
1	0	1	V0	V63	V0~V63	Black
1	1	0	GND	GND	V0~V63	White (With Flicker)
1	1	1	High impedance	High impedance	V0~V63	Abnormal (Crosstalk)

5.2.10. Frame Cycle Control (R0Ah)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	FMARKOE	FMI2	FMI1	FMI0

FMI [2:0]: (FMARK Interval) OTM3225C provide FMARK signal to prevent tearing effect. FMI [2:0] can set FMARK output interval.

FMI2	FMI1	FMI0	Output interval
0	0	0	1 frame
0	0	1	2 frames
0	1	0	3 frames
0	1	1	4 frames
1	0	0	5 frames
1	0	1	6 frames
1	1	0	7 frames
1	1	1	8 frames

FMARKOE: (FMARK Output Enable) Set the output signal FMARK from FMARK pin.

FMARK="0": Stop to output FMARK signal.

FMARK="1". Start to output FMARK signal.

5.2.11. External Display Interface Control 1 (R0Ch)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	ENC2	ENC1	ENC0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0

RIM1-0: To set the different transfer modes of RGB interface. **Table 5-12** summarized the function of RIM1-0 setting.

Table 5-12

RIM1	RIM0	RGB Interface Mode	Colors	Data Bus	Number of transfer during 1 line
0	0	18-bit RGB interface (one transfer/pixel)	262K	DB 17-0	240x18-bits (AM bit=0) 320x18-bits (AM bit=1)
0	1	16-bit RGB interface (one transfer/pixel)	65K	DB 17-13; DB 11-1	240x16-bits (AM bit=0) 320x16-bits (AM bit=1)
1	0	6-bit RGB interface (three transfers/pixel)	262K	DB17-12	720x6-bits (AM bit=0) 960x6-bits (AM bit=1)
1	1	8-bit RGB interface (two transfers/pixel)	65K	DB17-10	480x8-bits (AM bit=0) 640x8-bits (AM bit=1)

DM1-0: To specify the display interface mode. DM1-0 Setting can switch the display interface among system interface, RGB interface and VSYNC interface. **Table 5-13** summarized the function of DM1-0 setting.

Table 5-13

DM1	DM0	Display Interface
0	0	Internal clock operation
0	1	RGB interface
1	0	VSYNC interface
1	1	Setting disabled

RM: Select the interface to access the OTM3225C's internal GRAM. Set RM to "1" when writing display data via the RGB interface. The OTM3225C allows for setting the RM bit not constrained by the mode used for the display operation. This means it is possible to rewrite display data via a system interface by setting RM = "0" even while display operations are performed via the RGB interface.

Table 5-14 summarized the function of RM bit setting.

Table 5-14

RM	Interface for RAM Access
0	System interface/VSYNC interface
1	RGB interface

Table 5-15

Display State	Operation Mode	RAM access Mode(RM)	Display operation Mode (DM1-0)
Still pictures	Internal clock	System interface (RM = 0)	Internal clock operation (DM1-0 = 00)
Moving pictures	RGB interface	RGB interface (RM = 1)	RGB interface (DM1-0 = 01)
Rewrite still picture area while displaying moving pictures.	RGB interface	System interface (RM = 0)	RGB interface (DM1-0 = 01)
Moving pictures	VSYNC interface	System interface (RM = 0)	VSYNC interface (DM1-0 = 10)
Low Speed moving picture	RGB interface	RGB interface (RM = 1)	Internal clock operation (DM1-0 = 00)

Note1: Instructions are set only via the system interface.
Note2: Do not make changes to the RGB-I/F mode setting (RIM-0) while the RGB I/F is in operation.
Note3: See the "External Display Interface" section for the flowcharts to follow when switching from one mode to another.

5.2.12. Frame Maker Position (R0Dh)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	FMP8	FMP7	FMP6	FMP5	FMP4	FMP3	FMP2	FMP1	FMP0

FMP 8-0: Indicates the output position of frame cycle signal (FMARK).

A high-active pulse is output from FMARK pin and relate with back porch.

When FMP[8:0] =9'h000, FMARK is outputted at the start of back porch for 1line period.

When FMP[8:0] =9'h001, FMARK is outputted one line after the start of back porch.

Please reference section "FMARK function" for detail description.

FMP [8:0]	FMARK Output Position
9'h000	Immediate (Delay 0 line period)
9'h001	Delay 1 line period
9'h002	Delay 2 lines period
	~
Max. Vaule	9'h000≦FMP[8:0]≦BP+NL+FP

5.2.13. External Display Interface Control 2 (R0Fh)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	EPL	DPL

EPL: The polarity of ENABLE signal selection in RGB interface mode.

EPL = "0": ENABLE: Low active

EPL = "1": ENABLE: High active

DPL: Select the data latch edge of the DOTCLK signal in RGB interface mode.

DPL = "0": rising edge of the DOTCLK.

DPL ="1": falling edge of the DOTCLK.

VSPL: The polarity of VSYNC signal selection in RGB interface mode.

VSPL = "0": Low active.

VSPL = "1": High active.

HSPL: The polarity of HSYNC signal selection in RGB interface mode.

HSPL = "0": Low active.

HSPL = "1": High active.

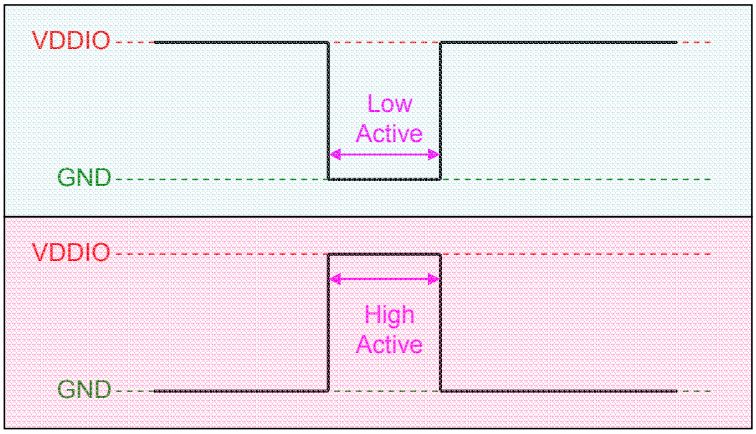


Figure 5-12

5.2.14. Power Control 1 (R10h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	SAP	0	BT2	BT1	BT0	APE	AP2	AP1	AP0	0	0	SLP	STB

SLP: Sleep mode selection. When SLP =1, OTM3225C set to sleep mode. In sleep mode, all internal operations are terminated including internal RC oscillation. Be sure that a display off sequence should be executed before set SLP to “1”. Set SLP=0 can exit sleep mode. Moreover, when exit from sleep mode, data in GRAM and in instruction registers are keep the same with these before set to SLP mode.

STB: Standby mode selection. When STB =1, OTM3225C set to standby mode. In this mode, all internal operations are terminated including internal RC oscillation. Be sure that a display off sequence should be executed before set STB to “1”. Set STB=0 can exit standby mode. Moreover, when exit from standby mode, data in GRAM and register will not lost, reset and re-sending command and data into GRAM is not necessary.

AP2-0: Operational amplifier DC bias current adjustment. Set AP2-0 = “000” to stop operational amplifier and DC/DC charge pump circuits to reduce current consumption during no display period.

APE: Enable bit for both liquid crystal power supply and gamma voltage generation circuit.

APE=”0”, Halt liquid crystal power supply and gamma voltage generation circuit.

APE=”1”, Enable liquid crystal power supply and gamma voltage generation circuit.

BT3-0: Set the voltage level of DDVDH, VGH, VGL and VCL.

Table 5-16 summarized the function of BT3-0 setting

BT2	BT1	BT0	DDVDH	VGH	VGL	VCL
0	0	0	VCI1 x 2	VCI1 x 6	VCI1x -5	-VCI1
0	0	1	VCI1 x 2	VCI1 x 6	VCI1x -4	-VCI1
0	1	0	VCI1 x 2	VCI1 x 6	VCI1x -3	-VCI1
0	1	1	VCI1 x 2	VCI1 x 5	VCI1x -5	-VCI1
1	0	0	VCI1 x 2	VCI1 x 5	VCI1x -4	-VCI1
1	0	1	VCI1 x 2	VCI1 x 5	VCI1x -3	-VCI1
1	1	0	VCI1 x 2	VCI1 x 4	VCI1x -4	-VCI1
1	1	1	VCI1 x 2	VCI1 x 4	VCI1x -3	-VCI1

SAP: Enable bit for gamma voltage generation circuit.

SAP=”0”, Halt gamma voltage generation circuit.

SAP=”1”, Enable gamma voltage generation circuit

5.2.15. Power Control 2 (R11h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	DC12	DC11	DC10	0	DC02	DC01	DC00	0	VC2	VC1	VC0

VC2-0: Set the voltage of VCIOUT. VCIOUT is generated by VCI. **Table 5-17** summarized the function of VC2-0 setting

Table 5-17

VC2	VC1	VC0	VCIOUT
0	0	0	0.95 x VCI
0	0	1	0.9 x VCI
0	1	0	0.85 x VCI
0	1	1	0.8 x VCI
1	0	0	0.75 x VCI
1	0	1	0.7 x VCI
1	1	0	0.65 x VCI
1	1	1	1.00 x VCI

DC02-00: Set DC/DC charge pump circuit 1 operating frequency. **Table 5-18** summarized the function of DC02-00 setting

Table 5-18

DC02	DC01	DC00	DC/DC charge pump circuit 1 frequency (fDCDC1)
0	0	0	2H
0	0	1	1H
0	1	0	1/2H
0	1	1	1/4H
1	0	0	1/8H
1	0	1	1/16H
1	1	0	1/32H
1	1	1	1/64H

DC12-10: Set DC/DC charge pump circuit 2 operating frequency. **Table 5- 19 s**ummarized the function of DC02-00 setting
Note: Be aware that DC/DC charge pump 1 frequency ≥ DC/DC charge pump 2 frequency

Table 5- 19

DC12	DC11	DC10	Step-up circuit 2 step-up frequency (fDCDC2)
0	0	0	1H
0	0	1	1/2H
0	1	0	1/4H
0	1	1	1/8H
1	0	0	1/16H
1	0	1	1/32H
1	1	0	1/64H
1	1	1	1/128H

Note: Be sure fDCDC1≥fDCDC2 when setting DC02-00, DC12-10.
CPU mode : 1H= Fosc / RTNI*DIVI
RGB mode : 1H= Fosc / RTNE*DIVE

5.2.16. Power Control 3 (R12h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	VCIRE	0	0	1	VRH3	VRH2	VRH1	VRH0

VCIRE: Select reference voltage for VREG1OUT

VCIRE = “0” (default): External VCI as reference voltage for VREG1OUT.

VCIRE = ”1”: Internal VCIR as reference voltage for VREG1OUT. (VCIR=2.5V)

VRH3-0: Set the voltage level of VCI. VCI is generated by VREG1OUT. **Table 5-20** summarized the function of VRH3-0 setting

Table 5-20

VRH3	VRH2	VRH1	VRH0	VREG1OUT voltage	
				VCIRE=0	VCIRE=1
0	0	0	0	Halt	Halt
0	0	0	1	VCIx2.00	2.5Vx2.00 = 5.000V
0	0	1	0	VCIx2.05	2.5Vx2.05 = 5.125V
0	0	1	1	VCIx2.10	2.5Vx2.10 = 5.250V
0	1	0	0	VCIx2.20	2.5Vx2.20 = 5.500V
0	1	0	1	VCIx2.30	2.5Vx2.30 = 5.750V
0	1	1	0	VCIx2.40	2.5Vx2.40 = 6.000V
0	1	1	1	VCIx2.40	2.5Vx2.40 = 6.000V
1	0	0	0	VCIx1.60	2.5Vx1.60 = 4.000V
1	0	0	1	VCIx1.65	2.5Vx1.65 = 4.125V
1	0	1	0	VCIx1.70	2.5Vx1.70 = 4.250V
1	0	1	1	VCIx1.75	2.5Vx1.75 = 4.375V
1	1	0	0	VCIx1.80	2.5Vx1.80 = 4.500V
1	1	0	1	VCIx1.85	2.5Vx1.85 = 4.625V
1	1	1	0	VCIx1.90	2.5Vx1.90 = 4.750V
1	1	1	1	VCIx1.95	2.5Vx1.95 = 4.875V

5.2.17. Power Control 4 (R13h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0

VDV4-0: Set the Vcom amplitude. Vcom amplitude is generated by VREG1OUT.

Table 5-21

VDV4	VDV3	VDV2	VDV1	VDV0	Vcom amplitude
0	0	0	0	0	VREG1OUT x 0.70
0	0	0	0	1	VREG1OUT x 0.72
0	0	0	1	0	VREG1OUT x 0.74
0	0	0	1	1	VREG1OUT x 0.76
0	0	1	0	0	VREG1OUT x 0.78
0	0	1	0	1	VREG1OUT x 0.80
0	0	1	1	0	VREG1OUT x 0.82
0	0	1	1	1	VREG1OUT x 0.84
0	1	0	0	0	VREG1OUT x 0.86
0	1	0	0	1	VREG1OUT x 0.88
0	1	0	1	0	VREG1OUT x 0.90
0	1	0	1	1	VREG1OUT x 0.92
0	1	1	0	0	VREG1OUT x 0.94
0	1	1	0	1	VREG1OUT x 0.96
0	1	1	1	0	VREG1OUT x 0.98
0	1	1	1	1	VREG1OUT x 1.00
1	0	0	0	0	VREG1OUT x 0.94
1	0	0	0	1	VREG1OUT x 0.96
1	0	0	1	0	VREG1OUT x 0.98
1	0	0	1	1	VREG1OUT x 1.00
1	0	1	0	0	VREG1OUT x 1.02
1	0	1	0	1	VREG1OUT x 1.04
1	0	1	1	0	VREG1OUT x 1.06
1	0	1	1	1	VREG1OUT x 1.08
1	1	0	0	0	VREG1OUT x 1.10
1	1	0	0	1	VREG1OUT x 1.12
1	1	0	1	0	VREG1OUT x 1.14
1	1	0	1	1	VREG1OUT x 1.16
1	1	1	0	0	VREG1OUT x 1.18
1	1	1	0	1	VREG1OUT x 1.20
1	1	1	1	0	VREG1OUT x 1.22
1	1	1	1	1	VREG1OUT x 1.24

5.2.18. GRAM Address Set (Horizontal Address) (R20h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

5.2.19. GRAM Address Set (Vertical Address) (R21h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8

AD16–0: To set the initial address counter for GRAM address. Based on AM and I/D[1:0] setting, the address counter is automatically increment or decrement while data are written to the internal GRAM. There is no need to updated AD16-0 every data transfer if AD16-0 was set in the beginning of one frame graphic data. Be aware that address counter is not automatically updated if reading data from the internal GRAM instruction is executed. Moreover, the address counter cannot be accessed when the OTM3225C is in standby mode.

Table 5-22 summarized the function of AD15-0 setting

Table 5-22

AD[16:0]	GRAM data map
17'h00000 – 17'h000EF	1st line GRAM data
17'h00100 –17'h001EF	2nd line GRAM data
17'h00200 –17'h002EF	3rd line GRAM data
17'h00300 –17'h003EF	4th line GRAM data
:	:
17'h13600 –17'h13CEF	317th line GRAM data
17'h13700 –17'h13DEF	318th line GRAM data
17'h13800 –17'h13EEF	319th line GRAM data
17'h13900 –17'h13FEF	320th line GRAM data

5.2.20. Write Data to GRAM (R22h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	RAM write data (WD17-0) The DB17-0 pin assignment is different in different interface modes.															

WD17-0: OTM3225C supports 18 bits data format. However, if only 16-bit (565format) is input to GRAM, OTM3225C will expand the 16 bit data into 18-bit format. Same case when RGB interface is selected. Based on the graphic data in GRAM, the grayscale voltage of source driver is selected. **Table 5-23** summarized the source driver grayscale voltage output versus graphic data in GRAM. **Figure 5-13 ~Figure 5-26** illustrates the pin assignment among data bus (DB17-0), R22 (WD17-0) and GRAM.

Table 5-23

Data in GRAM	Source Driver Grayscale Output	
RGB	Negative	Positive
000000	V0	V63
000001	V1	V62
000010	V2	V61
000011	V3	V60
000100	V4	V59
000101	V5	V58
000110	V6	V57
000111	V7	V56
001000	V8	V55
001001	V9	V54
001010	V10	V53
001011	V11	V52
001100	V12	V51
001101	V13	V50
001110	V14	V49
001111	V15	V48
010000	V16	V47
010001	V17	V46
010010	V18	V45
010011	V19	V44
010100	V20	V43
010101	V21	V42
010110	V22	V41
010111	V23	V40
011000	V24	V39
011001	V25	V38
011010	V26	V37
011011	V27	V36
011100	V28	V35
011101	V29	V34
011110	V30	V33
011111	V31	V32
100000	V32	V31
100001	V33	V30
100010	V34	V29
100011	V35	V28
100100	V36	V27
100101	V37	V26
100110	V38	V25
100111	V39	V24
101000	V40	V23
101001	V41	V22
101010	V42	V21
101011	V43	V20
101100	V44	V19
101101	V45	V18
101110	V46	V17
101111	V47	V16
110000	V48	V15
110001	V49	V14
110010	V50	V13
110011	V51	V12
110100	V52	V11
110101	V53	V10
110110	V54	V9
110111	V55	V8
111000	V56	V7
111001	V57	V6
111010	V58	V5
111011	V59	V4
111100	V60	V3
111101	V61	V2
111110	V62	V1
111111	V63	V0

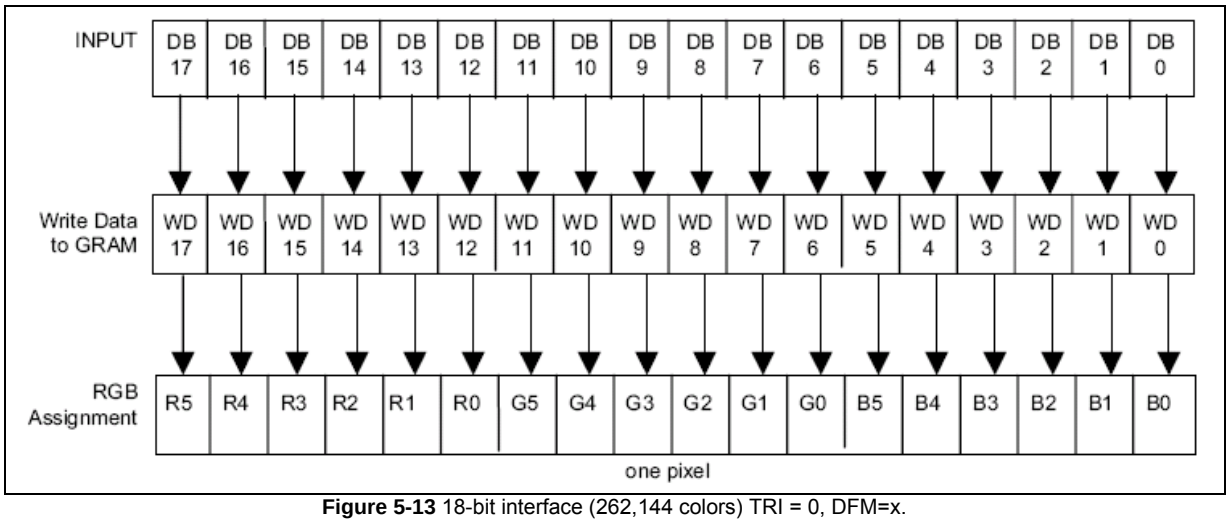


Figure 5-13 18-bit interface (262,144 colors) TRI = 0, DFM=x.

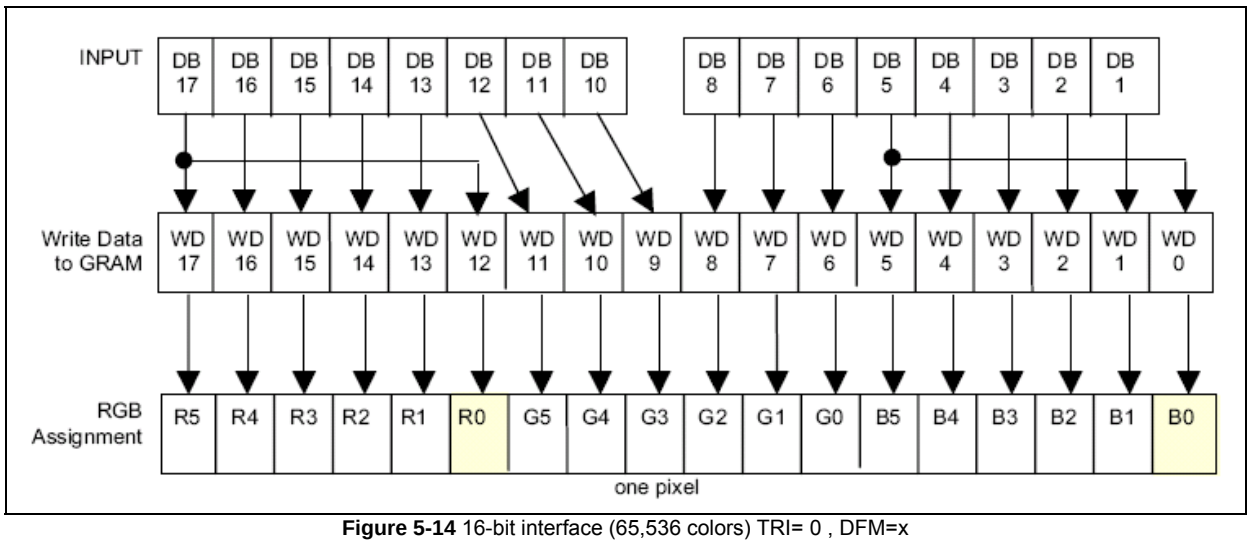


Figure 5-14 16-bit interface (65,536 colors) TRI= 0 , DFM=x

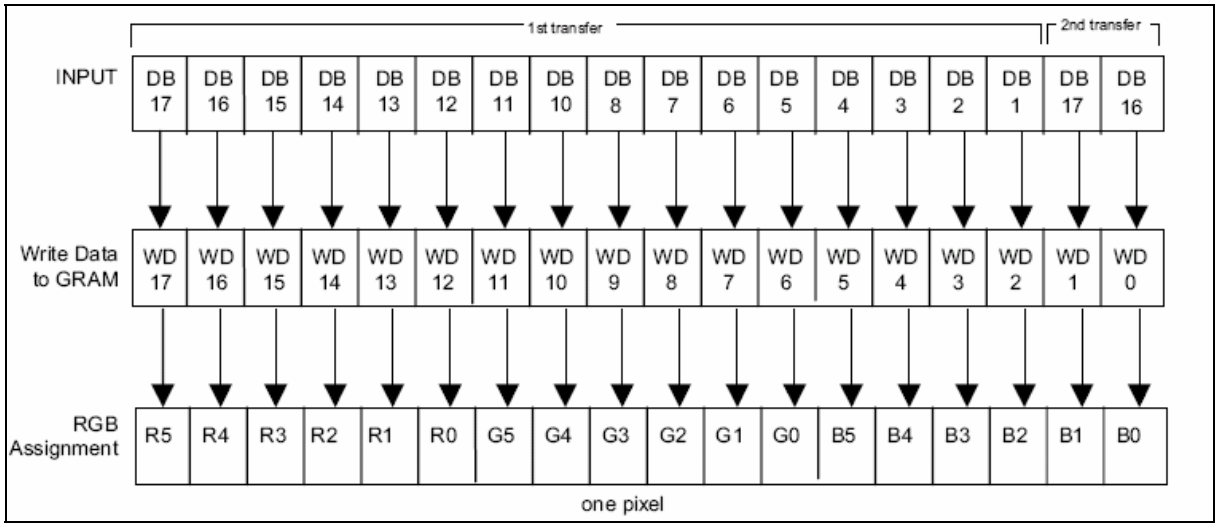


Figure 5-15 16-bit interface (262,144 colors) TRI = 1, DFM = 0

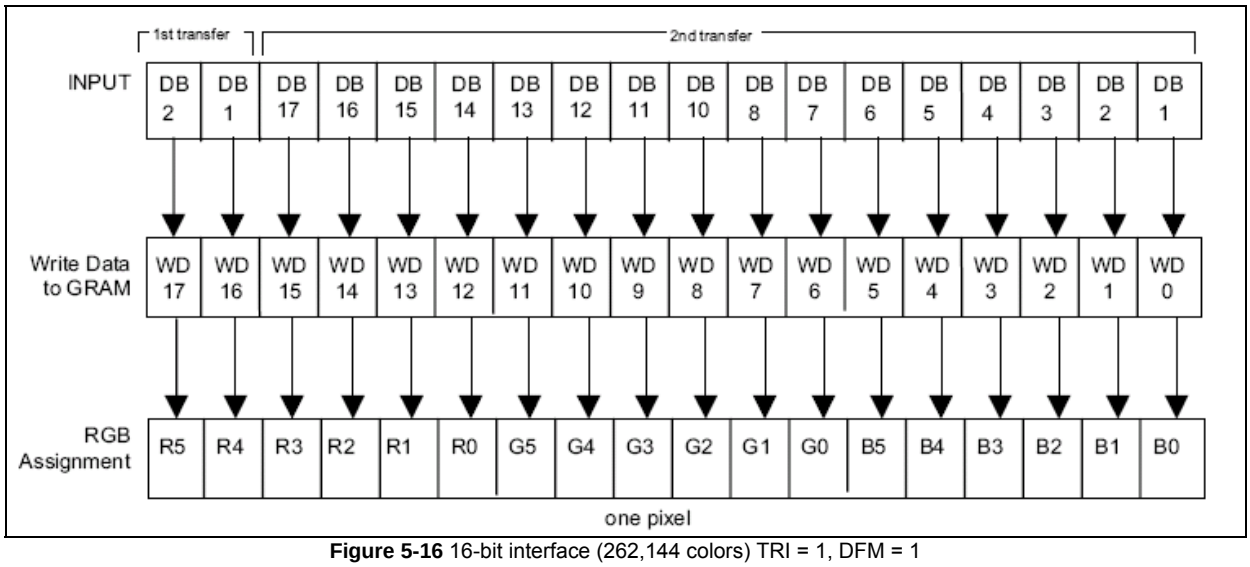


Figure 5-16 16-bit interface (262,144 colors) TRI = 1, DFM = 1

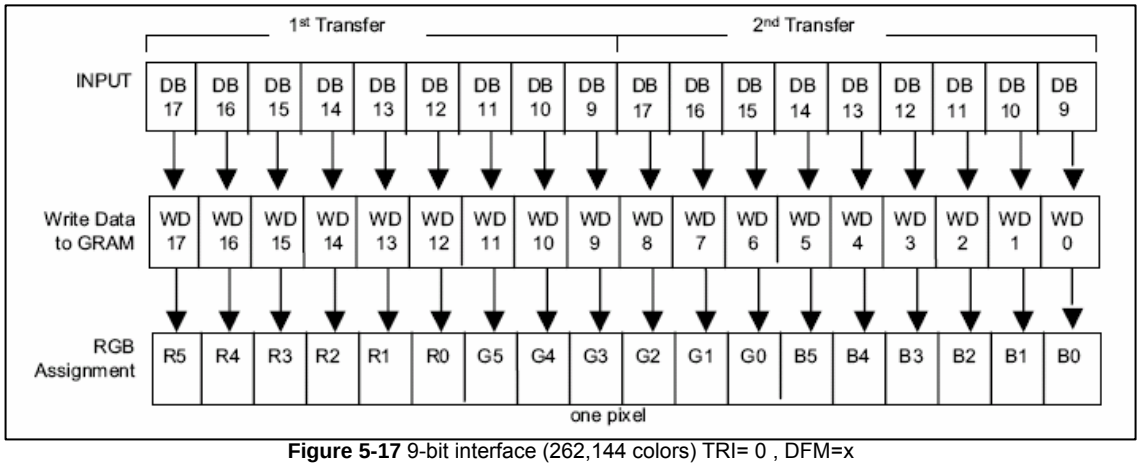


Figure 5-17 9-bit interface (262,144 colors) TRI= 0 , DFM=x

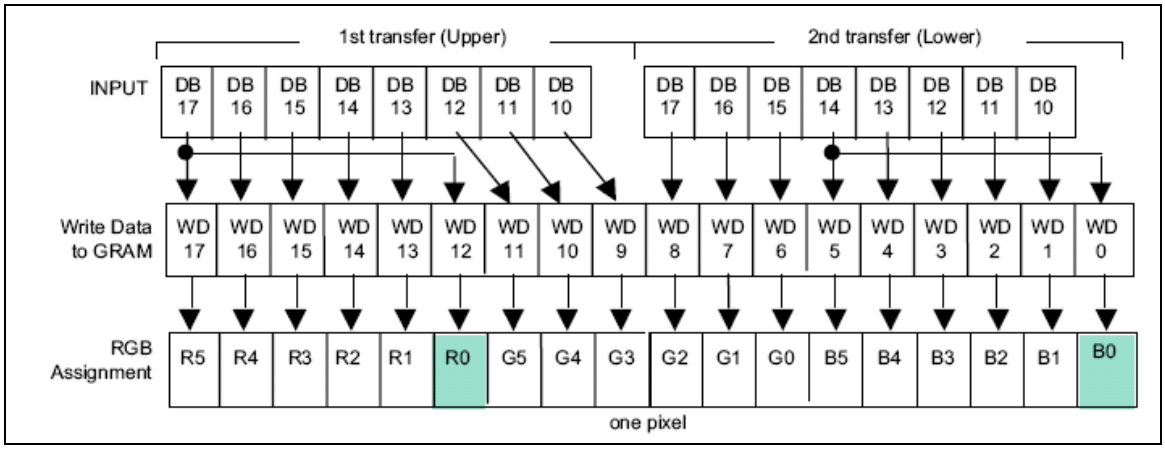


Figure 5-18 8-bit interface (65,536 colors) TRI = 0, DFM=x

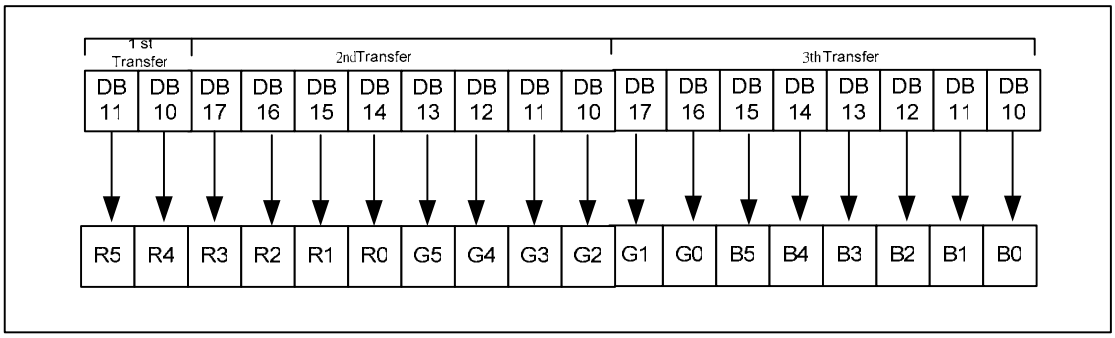


Figure 5-19 8-bit interface (262,144 colors) TRI = 1, DFM=0.

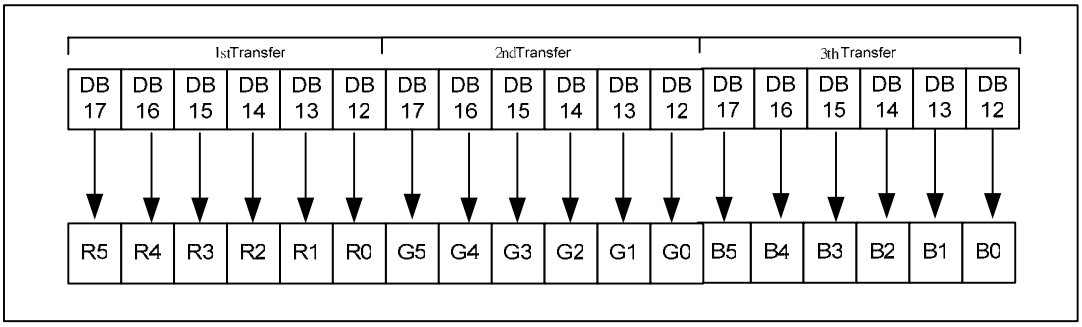


Figure 5-20 8-bit interface (262,144 colors) TRI = 1, DFM=1

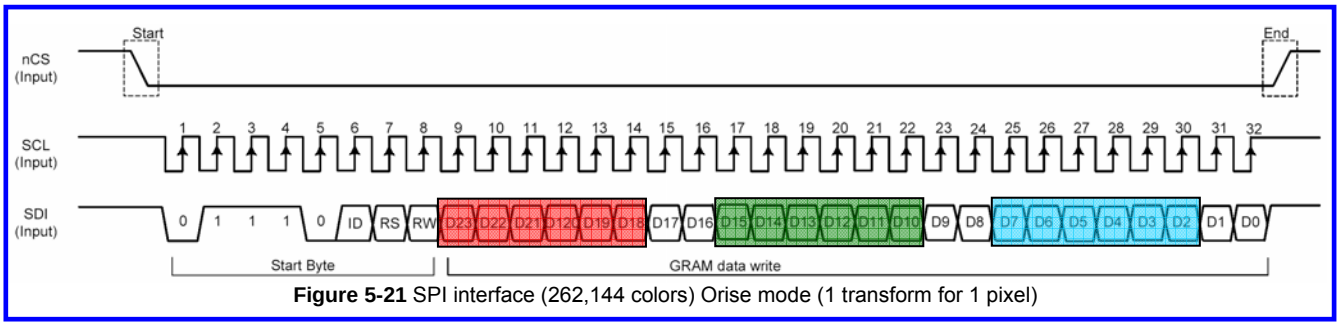


Figure 5-21 SPI interface (262,144 colors) Orise mode (1 transform for 1 pixel)

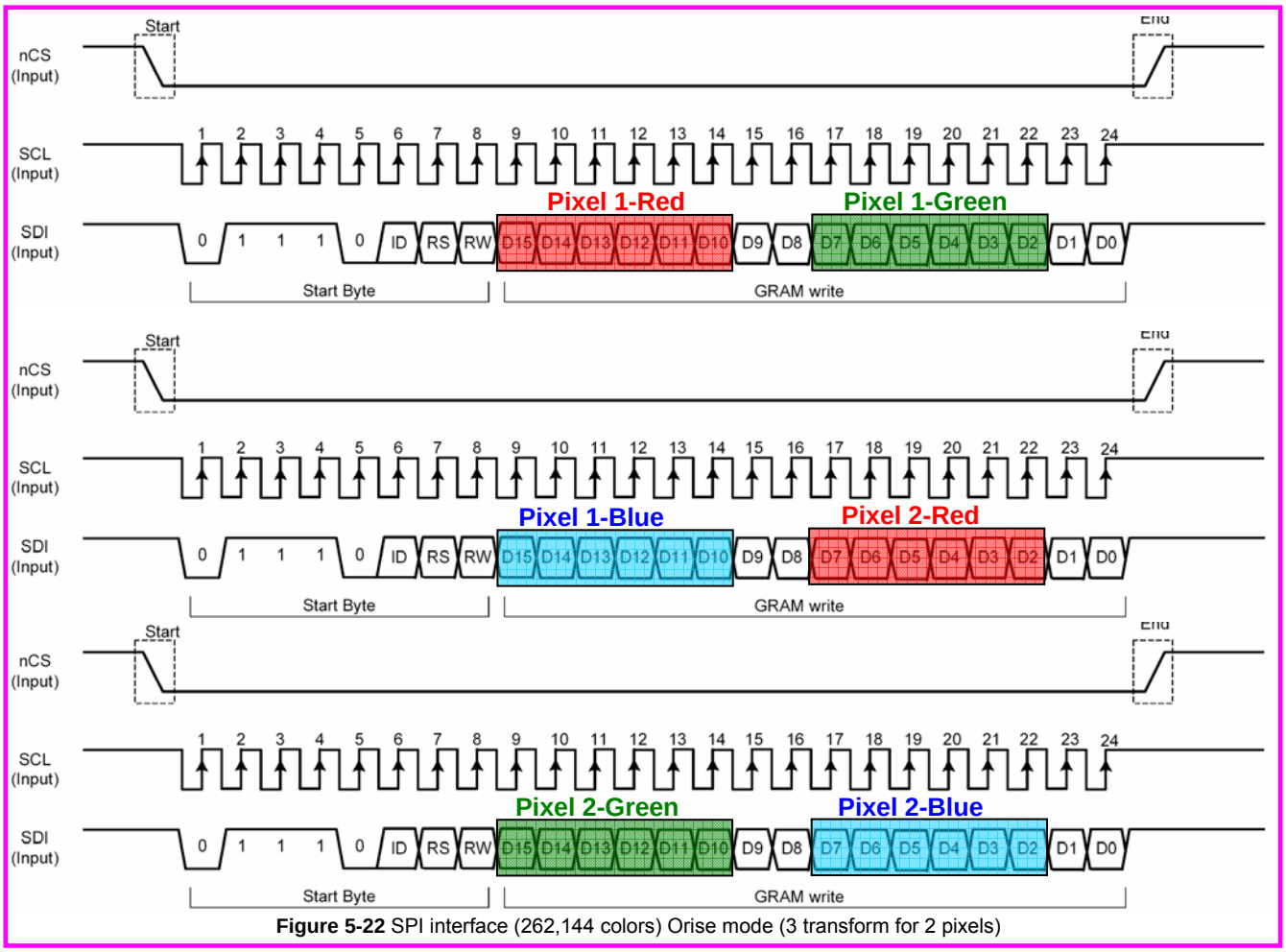


Figure 5-22 SPI interface (262,144 colors) Orise mode (3 transform for 2 pixels)

★**Orise Mode:** Please contact OriseTech and request the initial code for the SPI 262K mode.

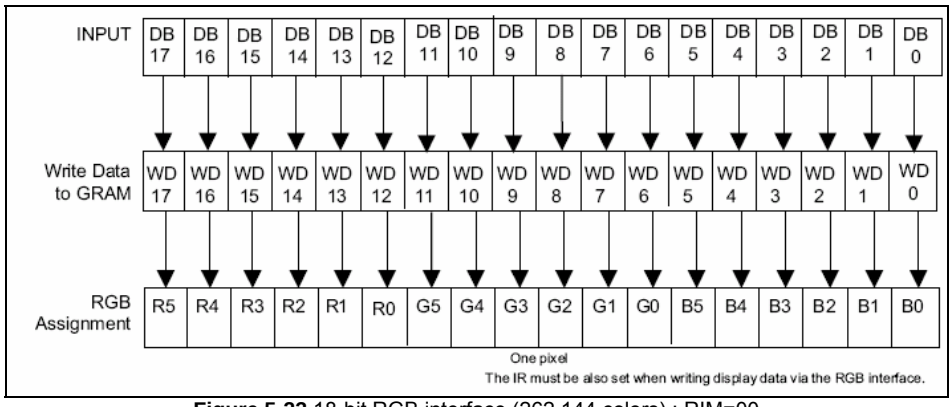


Figure 5-23 18-bit RGB interface (262,144 colors) ; RIM=00

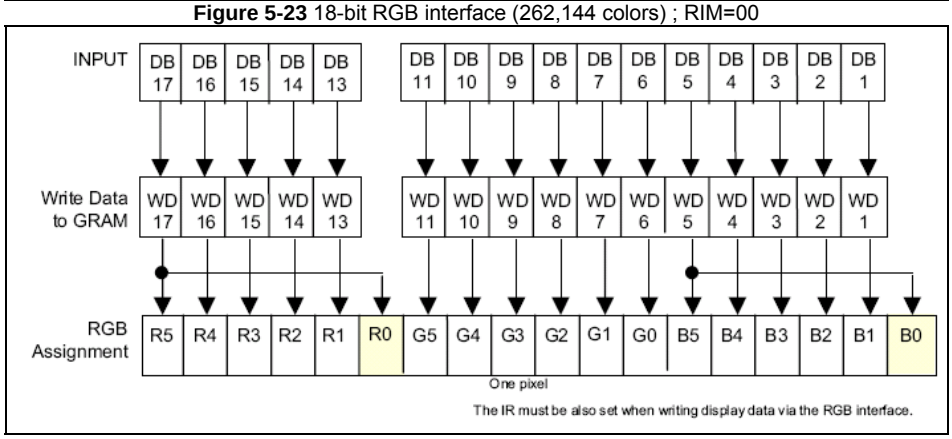


Figure 5-24 16-bit RGB interface (65,563 colors) ; RIM=01

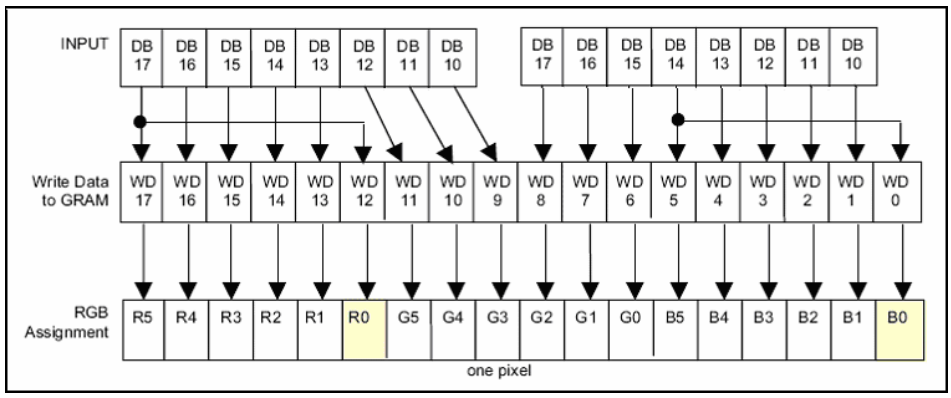


Figure 5-25 8-bit RGB interface (65,563 colors) ; RIM=11

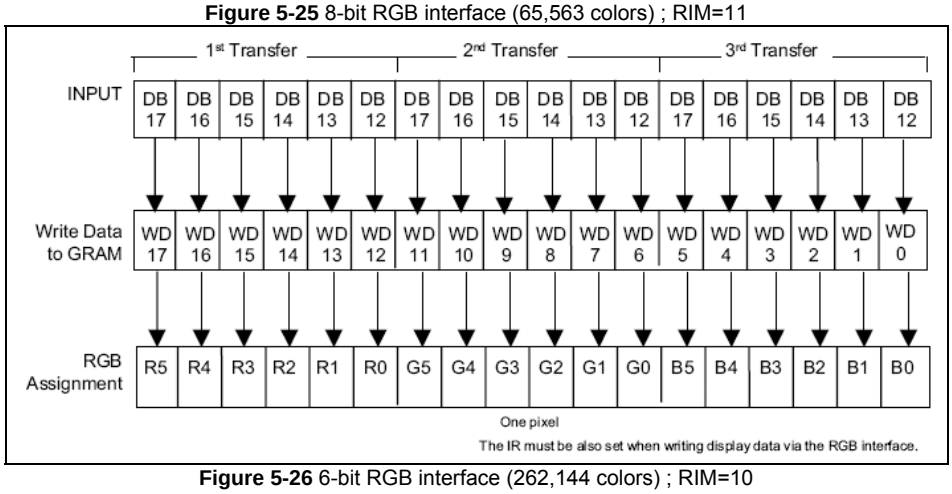


Figure 5-26 6-bit RGB interface (262,144 colors) ; RIM=10

OTM3225C supports external (RGB) interface. In RGB interface mode, all graphic data are stored in GRAM. To meet the diverse requirement of small size LCD panel, OTM3225C also supports in a fix window using RGB interface and outside the window still use system interface.

In RGB interface mode, data writing to the internal RAM is synchronized with DOTCLK during ENABLE = “Low”. Set ENABLE “High” to terminate writing data to RAM. Wait for a write/read bus cycle time. If accessing internal RAM using the RGB interface is desired after accessing the RAM via the system interface. **Figure 5-27** illustrates the timing diagram while RGB and system interface are both use in the same time.

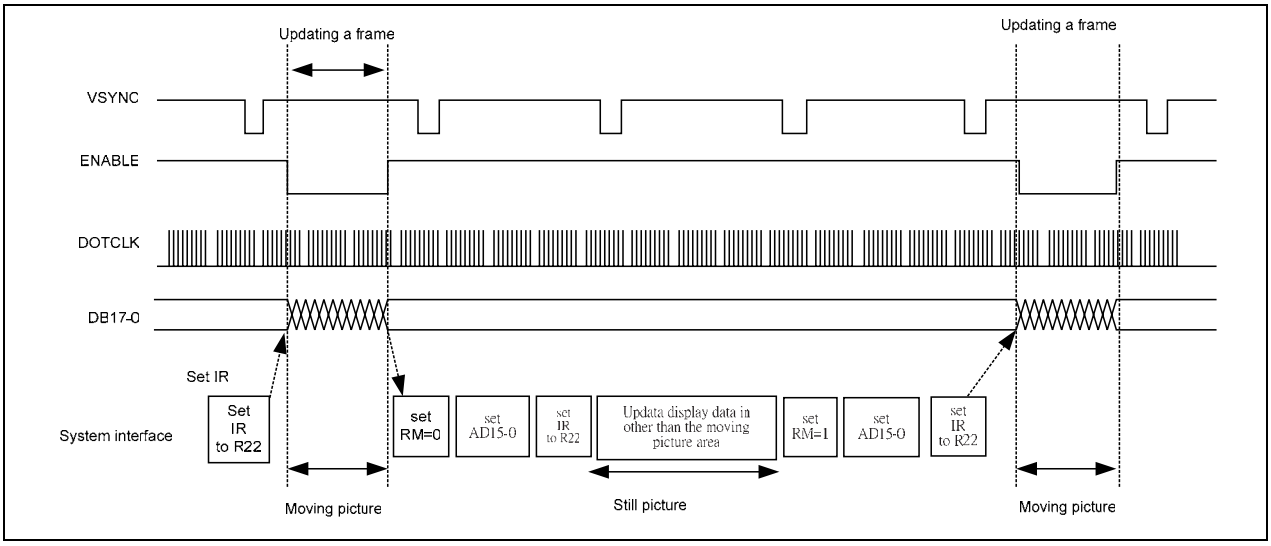


Figure 5-27

5.2.21. Read Data Read from GRAM (R22h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
R	1	RAM Read data (RD17-0) The DB17-0 pin assignment is different in different interface modes.															

R22 also served as a register, which store the data read out from GRAM. When data are read out from the GRAM is desired, first sets the RAM address and executes first word read, and issues second word read. When first word read instruction is issued, Invalid data are sent to the data bus DB17-0. Valid data are sent to the data bus as second word data is executed.

Note 1: The LSBs of R and B dots cannot read out, when the 8 or 16-bit interface is selected,

Note 2: This register is not available with the RGB interface. **Figure 5-28 ~ Figure 5-31** illustrates the pin assignment among data bus (DB17-0), R22 (RD17-0) and GRAM in read data instruction.

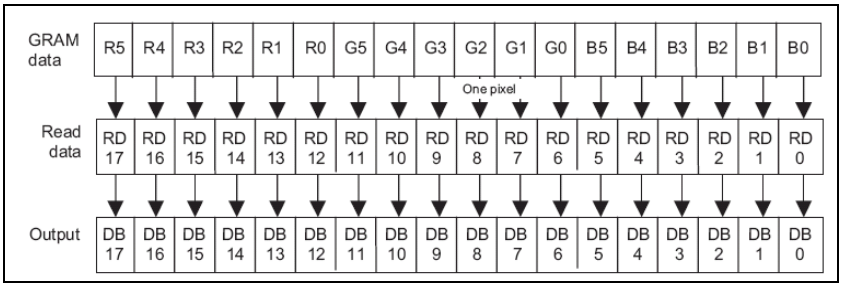


Figure 5-28 18-bit interface

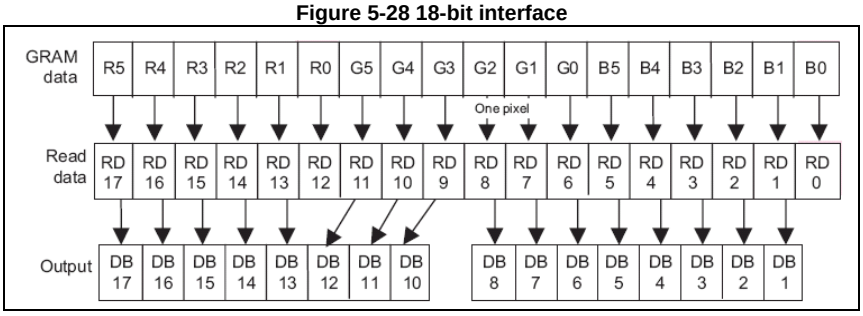


Figure 5-29 16-bit interface

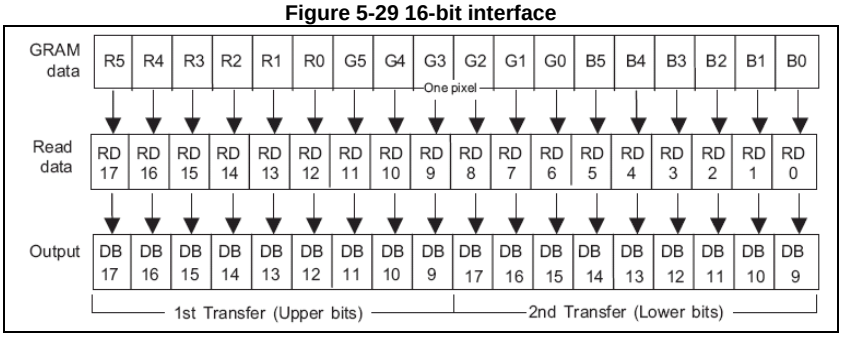


Figure 5-30 9-bit interface

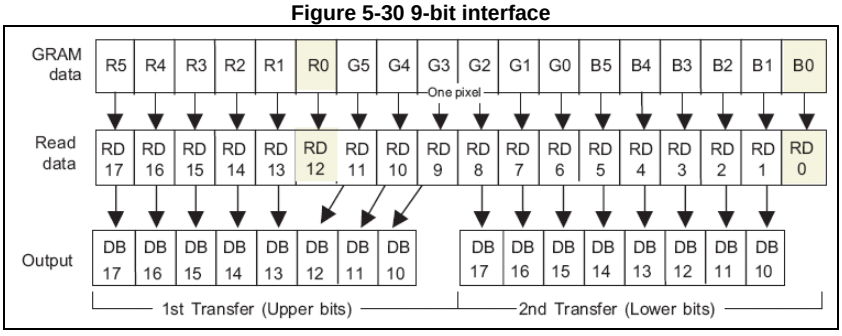


Figure 5-31 8-bit interface / SPI(65K color)

5.2.22. Power Control 7 (R29h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0

VCM [5:0]: These pins are to set the factor for generating VCOMH.

Table 5-24 summarized the factor of VERG1OUT

Table 5-24

VCM[5:0]	VCOMH voltage
6'h00	VREG1OUT x 0.685
6'h01	VREG1OUT x 0.690
6'h02	VREG1OUT x 0.695
6'h03	VREG1OUT x 0.700
6'h04	VREG1OUT x 0.705
6'h05	VREG1OUT x 0.710
6'h06	VREG1OUT x 0.715
6'h07	VREG1OUT x 0.720
6'h08	VREG1OUT x 0.725
6'h09	VREG1OUT x 0.730
6'h0A	VREG1OUT x 0.735
6'h0B	VREG1OUT x 0.740
6'h0C	VREG1OUT x 0.745
6'h0D	VREG1OUT x 0.750
6'h0E	VREG1OUT x 0.755
6'h0F	VREG1OUT x 0.760
6'h10	VREG1OUT x 0.765
6'h11	VREG1OUT x 0.770
6'h12	VREG1OUT x 0.775
6'h13	VREG1OUT x 0.780
6'h14	VREG1OUT x 0.785
6'h15	VREG1OUT x 0.790
6'h16	VREG1OUT x 0.795
6'h17	VREG1OUT x 0.800
6'h18	VREG1OUT x 0.805
6'h19	VREG1OUT x 0.810
6'h1A	VREG1OUT x 0.815
6'h1B	VREG1OUT x 0.820
6'h1C	VREG1OUT x 0.825
6'h1D	VREG1OUT x 0.830
6'h1E	VREG1OUT x 0.835
6'h1F	VREG1OUT x 0.840

VCM[5:0]	VCOMH voltage
6'h20	VREG1OUT x 0.845
6'h21	VREG1OUT x 0.850
6'h22	VREG1OUT x 0.855
6'h23	VREG1OUT x 0.860
6'h24	VREG1OUT x 0.865
6'h25	VREG1OUT x 0.870
6'h26	VREG1OUT x 0.875
6'h27	VREG1OUT x 0.880
6'h28	VREG1OUT x 0.885
6'h29	VREG1OUT x 0.890
6'h2A	VREG1OUT x 0.895
6'h2B	VREG1OUT x 0.900
6'h2C	VREG1OUT x 0.905
6'h2D	VREG1OUT x 0.910
6'h2E	VREG1OUT x 0.915
6'h2F	VREG1OUT x 0.920
6'h30	VREG1OUT x 0.925
6'h31	VREG1OUT x 0.930
6'h32	VREG1OUT x 0.935
6'h33	VREG1OUT x 0.940
6'h34	VREG1OUT x 0.945
6'h35	VREG1OUT x 0.950
6'h36	VREG1OUT x 0.955
6'h37	VREG1OUT x 0.960
6'h38	VREG1OUT x 0.965
6'h39	VREG1OUT x 0.970
6'h3A	VREG1OUT x 0.975
6'h3B	VREG1OUT x 0.980
6'h3C	VREG1OUT x 0.985
6'h3D	VREG1OUT x 0.990
6'h3E	VREG1OUT x 0.995
6'h3F	VREG1OUT x 0.1000

5.2.23. Frame rate control (R2Bh)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	FRS3	FRS2	FRS1	FRS0

FRS[4:0] Set the oscillator frequency to change frame rate.

Table 5-25 summarized the oscillator frequency and the frame rate.

Note 1: The frame rate is relative to DIVI[1:0] ; RTNI[4:0] ; NL[5:0] ; BP[3:0] and FP[3:0] bits.

Table 5-25 (BP+FP=9; RTNI=0 ; DIVI=0)

FRS[3:0]	OSC frequency	Frame rate
6'h00	375K	30 Hz
6'h01	387K	31 Hz
6'h02	413K	33 Hz
6'h03	437K	35 Hz
6'h04	475K	38 Hz
6'h05	500K	40 Hz
6'h06	537K	43 Hz
6'h07	587K	47 Hz

FRS[3:0]	OSC frequency	Frame rate
6'h08	637K	51 Hz
6'h09	700K	56 Hz
6'h0A	775K	62 Hz
6'h0B	875K	70 Hz
6'h0C	1000K	80 Hz
6'h0D	1162K	93 Hz
6'h0E	1400K	112 Hz
6'h0F	1400K	112 Hz

Formula to calculate frame frequency

$$Frame\ frequency = \frac{fosc}{Clock\ cycles\ per\ line \times Division\ ratio \times (Line + BP + LP)} \quad [\text{Hz}]$$

fosc: frequency of RC oscillator (FRS bits)

Line: number of lines for driving liquid crystal (NL bits)

Division ratio: DIVI bits

Clock cycles per line: RTNI bits

FP: the number of lines for the front porch period (FP bits)

BP: the number of lines for the back porch period (BP bits)

5.2.24. γ Control (R30h to R3Dh)

	R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
R30	W	1	0	0	0	0	0	KP1[2]	KP1[1]	KP1[0]	0	0	0	0	0	KP0[2]	KP0[1]	KP0[0]
R31	W	1	0	0	0	0	0	KP3[2]	KP3[1]	KP3[0]	0	0	0	0	0	KP2[2]	KP2[1]	KP2[0]
R32	W	1	0	0	0	0	0	KP5[2]	KP5[1]	KP5[0]	0	0	0	0	0	KP4[2]	KP4[1]	KP4[0]
R35	W	1	0	0	0	0	0	RP1[2]	RP1[2]	RP1[0]	0	0	0	0	0	RP0[2]	RP0[2]	RP0[0]
R36	W	1	0	0	0	VRP1[4]	VRP1[3]	VRP1[2]	VRP1[1]	VRP1[0]	0	0	0	VRP0[4]	VRP0[3]	VRP0[2]	VRP0[1]	VRP0[0]
R37	W	1	0	0	0	0	0	KN1[2]	KN1[1]	KN1[0]	0	0	0	0	0	KN0[2]	KN0[1]	KN0[0]
R38	W	1	0	0	0	0	0	KN3[2]	KN3[1]	KN3[0]	0	0	0	0	0	KN2[2]	KN2[1]	KN2[0]
R39	W	1	0	0	0	0	0	KN5[2]	KN5[1]	KN5[0]	0	0	0	0	0	KN4[2]	KN4[1]	KN4[0]
R3C	W	1	0	0	0	0	0	RN1[2]	RN1[1]	RN1[0]	0	0	0	0	0	RN0[2]	RN0[1]	RN0[0]
R3D	W	1	0	0	0	VRN1[4]	VRN1[3]	VRN1[2]	VRN1[1]	VRN1[0]	0	0	0	VRN0[4]	VRN0[3]	VRN0[2]	VRN0[1]	VRN0[0]

γ **Control (R30h to R3Dh):** OTM3225C provides 10 gamma registers to fine tune gamma output voltage.

KP5-0[2:0]: γ **fine tune** registers for positive polarity.
RP1-0[2:0]: γ **gradient** registers for positive polarity.
VRP1-0[4:0]: γ **amplitude** registers for positive polarity.
KN5-0[2:0]: γ **fine tune** registers for positive polarity.
RN1-0[2:0]: γ **gradient** registers for positive polarity.
VRN1-0[4:0]: γ **amplitude** registers for positive polarity.

5.2.25. Window Horizontal RAM Address Start (R50h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0

5.2.26. Window Horizontal RAM Address End (R51h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0

5.2.27. Window Vertical RAM Address Start (R52h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0

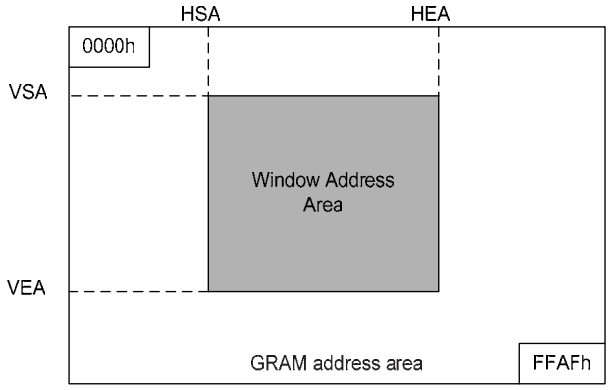
5.2.28. Window Vertical RAM Address End (R53h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	VEA8	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0

HSA7-0/HEA7-0: OTM3225C provides window access function. Set HSA7-0 and HEA7-0 represent the start address and end address of the window function in horizontal direction. To use window-accessing function, HSA and HEA bits must be set before starting RAM write operation. Be aware that “00”h ≤ HSA7-0< HEA7-0 ≤ “EF”h and HEA-HSA>=”01h”.

VSA8-0/VEA8-0: OTM3225C provides window access function. Set VSA8-0 and VEA8-0 represent the start address and end address of the window in vertical direction. To use window accessing function, VSA and VEA bits must be set before starting RAM write operation. Be aware that “00”h ≤ VSA8-0< VEA8-0 ≤ 9’h13F.

Figure 5-32. illustrates the window-accessing function using R50h~R53h.



5.2.29. Gate Driver Scan Control (R60h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	GS	0	NL5	NL4	NL3	NL2	NL1	NL0	0	0	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0

SCN5-0: Set the SCN5-0 bits can specify the starting position of the gate driver. The start position of gate driver is determined by the combination of the setting of GS and SM.

Table 5-26 summarized the starting position for each SCN5-0 setting.

Table 5-26

SCN[5:0]	Scan Start Position (Gate line)			
	SM=0		SM=1	
	GS = "0"	GS = "1"	GS = "0"	GS = "1"
6'h00	G1	G320	G1	G320
6'h01	G9	G312	G17	G304
6'h02	G17	G304	G33	G288
6'h03	G25	G296	G49	G272
6'h04	G33	G288	G65	G256
6'h05	G41	G280	G81	G240
6'h06	G49	G272	G97	G224
6'h07	G57	G264	G113	G208
6'h08	G65	G256	G129	G192
6'h09	G73	G248	G145	G176
6'h0A	G81	G240	G161	G160
6'h0B	G89	G232	G177	G144
6'h0C	G97	G224	G193	G128
6'h0D	G105	G216	G209	G112
6'h0E	G113	G208	G2	G96
6'h0F	G121	G200	G18	G80
6'h10	G129	G192	G34	G64
6'h11	G137	G184	G50	G48
6'h12	G145	G176	G66	G32
6'h13	G153	G168	G82	G16
6'h14	G161	G160	G98	G319
6'h15	G169	G152	G114	G303
6'h16	G177	G144	G130	G287
6'h17	G185	G136	G146	G271
6'h18	G193	G128	G162	G255
6'h19	G201	G120	G178	G239
6'h1A	G209	G112	G194	G223
6'h1B	G217	G104	G114	G207
6'h1C	G225	G96	G130	G191
6'h1D	G233	G88	G146	G175
6'h1E	G241	G80	G162	G159
6'h1F	G249	G72	G178	G143
6'h20	G257	G64	G194	G127
6'h21	G265	G56	G210	G111
6'h22	G273	G48	G226	G95
6'h23	G281	G40	G242	G79
6'h24	G289	G32	G258	G63
6'h25	G297	G24	G274	G47
6'h26	G305	G16	G290	G31
6'h27	G313	G8	G306	G15
6'h28~3F	Setting disabled			

NL5-0: Set the number of gate lines for different resolution of display panel. The combination of NL5-NL0 represents the gate line number are summarized at **Table 5-27**.

Table 5-27

NL[5:0]	Display Size	Drive lines
6'h00	720 x 8 dots	8
6'h01	720 x 16 dots	16
6'h02	720 x 24 dots	24
…	…	…
6'h1F	720 x 256 dots	256
6'h20	720 x 264 dots	264
6'h21	720 x 272 dots	272
6'h22	720 x 280 dots	280
6'h23	720 x 288 dots	288
6'h24	720 x 296 dots	296
6'h25	720 x 304 dots	304
6'h26	720 x 312 dots	312
6'h27	720 x 320 dots	320

Note 1: Be sure that NL[5:0]≧SCN[5:0].

Note 2: Be sure that NL[5:0]≦6'h27.

GS: Shift direction of the gate driver output selection. When
GS="0", gate driver shift from G1 to G320. When GS = "1", gate driver shift from G320 to G1.

5.2.30. Driver Output Control (R61h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV

REV: To set the grayscale corresponding to normally white or normally black LCD panel from same data input.

Table 5-28 summarized REV bit function.

Table 5-28

REV	GRAM data	Source Driver Output	
		Positive Polarity	Negative Polarity
0	18'h00000 ⋮ 18'h3FFFF	V63 ⋮ V0	V0 ⋮ V63
1	18'h00000 ⋮ 18'h3FFFF	V0 ⋮ V63	V63 ⋮ V0

VLE: OTM3225C provides vertical scrolling function which can be set by VLE bit.

VLE = "1", vertical scrolling function enable. The amount of scrolling line from the first line is determined by VL[8:0].

VLE = "0", normal display.

NDL: set the source diver output level in non-lit area..

NDL = "1", .

NDL = "0", .

5.2.31. Vertical Scroll Control (R6Ah)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0

VL8-0: OTM3225C provides scrolling function. The start position for displaying the image is shifted vertically by the number of lines based on the setting of the VL8-0 bits. Be aware that the vertical scrolling function is not available in the external (RGB) display interface mode. **Table 5-29** summarized the function of VL8-0 setting.

Table 5-29

VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	Scrolling lines
0	0	0	0	0	0	0	0	0	0 line
0	0	0	0	0	0	0	0	1	1 line
0	0	0	0	0	0	0	1	0	2 lines
	:	:	:	:	:	:	:	:	:
1	0	0	1	1	1	1	1	1	319 lines
1	0	1	0	0	0	0	0	0	320 lines

Note 1: Be sure that VL[8:0]≦9'h140.

5.2.32. Display Position – Partial Display 1 (R80h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	PTDP08	PTDP07	PTDP06	PTDP05	PTDP04	PTDP03	PTDP02	PTDP01	PTDP00

5.2.33. RAM Address Start – Partial Display 1 (R81h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	PTSA08	PTSA07	PTSA06	PTSA05	PTSA04	PTSA03	PTSA02	PTSA01	PTSA00

5.2.34. RAM Address End – Partial Display 1 (R82h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	PTEA08	PTEA07	PTEA06	PTEA05	PTEA04	PTEA03	PTEA02	PTEA01	PTEA00

5.2.35. Display Position – Partial Display 2 (R83h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	PTDP18	PTDP17	PTDP16	PTDP15	PTDP14	PTDP13	PTDP12	PTDP11	PTDP10

5.2.36. RAM Address Start – Partial Display 2 (R84h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	PTSA18	PTSA17	PTSA16	PTSA15	PTSA14	PTSA13	PTSA12	PTSA11	PTSA10

5.2.37. RAM Address End – Partial Display 2 (R85h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	PTEA18	PTEA17	PTEA16	PTEA15	PTEA14	PTEA13	PTEA12	PTEA11	PTEA10

PTDP0[8:0]: Set the physical starting position of partial display 1 on the LCD panel

PTDP1[8:0]: Set the physical starting position of partial display 2 on the LCD panel

The partial display 1 and partial display 2 should not overlap with each other. And make sure the PTDP0[8:0] < PTDP1[8:0].

PTSA0[8:0]: Set the start line address of display RAM of partial display 1 which will be display according to PTDP0[8:0].

PTEA0[8:0]: Set the end line address of display RAM of partial display 1 which will be display according to PTDP0[8:0].

Note 1: Make sure PTSA0<=PTEA0

PTSA1[8:0]: Set the start line address of display RAM of partial display2 which will be display according to PTDP1[8:0].

PTEA1[8:0]: Set the end line address of display RAM of partial display2 which will be display according to PTDP1[8:0]

Note 1: Make sure PTSA1<=PTEA1

5.2.38. Panel Interface Control 1 (R90h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	DIVI1	DIVI0	0	0	0	RTNI4	RTNI 3	RTNI 2	RTNI 1	RTNI 0

RTNI4-0: Set the clock cycle per line **Table 5-30** summarized the function of RTNI4-0 setting.

Table 5-30

RTNI4	RTNI3	RTNI2	RTNI1	RTNI0	Clock Cycles per line
0	0	0	0	0	38 clocks
0	0	0	0	1	40 clocks
0	0	0	1	0	42 clocks
0	0	0	1	1	44 clocks
0	0	1	0	0	46 clocks
0	0	1	0	1	48 clocks
0	0	1	1	0	50 clocks
0	0	1	1	1	52 clocks
0	1	0	0	0	54 clocks
0	1	0	0	1	56 clocks
0	1	0	1	0	58 clocks
0	1	0	1	1	60 clocks
0	1	1	0	0	62 clocks
0	1	1	0	1	64 clocks
0	1	1	1	0	66 clocks
0	1	1	1	1	68 clocks
1	0	0	0	0	38 clocks
1	0	0	0	1	40 clocks
1	0	0	1	0	42 clocks
1	0	0	1	1	44 clocks
1	0	1	0	0	46 clocks
1	0	1	0	1	48 clocks
1	0	1	1	0	50 clocks
1	0	1	1	1	52 clocks
1	1	0	0	0	54 clocks
1	1	0	0	1	56 clocks
1	1	0	1	0	58 clocks
1	1	0	1	1	60 clocks
1	1	1	0	0	62 clocks
1	1	1	0	1	64 clocks
1	1	1	1	0	66 clocks
1	1	1	1	1	68 clocks

DIVI1-0: To specified the division ratio of internal operation clock frequency. Set the RTNI and DIVI bits to adjust frame frequency. Be aware of that if the number of lines for driving liquid crystal is changed, the frame frequency must also be adjusted. Moreover, In RGB interface mode, the DIVI1-0 bits are disabled. **Table 5-31** summarized the function of DIVI1-0 setting.

Table 5-31

DIVI1	DIVI0	Division Ratio	Internal Operation Clock Frequency
0	0	1	fosc / 1
0	1	2	fosc / 2
1	0	4	fosc / 4
1	1	8	fosc / 8

5.2.39. Panel Interface Control 2 (R92h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	NOWI2	NOWI1	NOWI0	0	0	0	0	0	0	0	0

NOWI [2:0]: Set the adjacent gate driver output non-overlap period. **Table 5-32** summarized the function of NOWI2-0 setting.

Table 5-32

NOWI2	NOWI1	NOWI0	Gate output non-overlap period Internal Operation (reference clock: internal oscillator)
0	0	0	2 clocks
0	0	1	2 clocks
0	1	0	4 clocks
0	1	1	6 clocks
1	0	0	8 clocks
1	0	1	10 clocks
1	1	0	12 clocks
1	1	1	14 clocks

5.2.40. Panel Interface control 4 (R95h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	DIVE1	DIVE0	0	0	RTNE5	RTNE4	RTNE3	RTNE2	RTNE1	RTNE0

RTNE5-0: Set the clock cycle per line **Table 5-33** summarized the function of RTNE5-0 setting.

Table 5-33

RTNE5	RTNE4	RTNE3	RTNE2	RTNE1	RTNE0	Clock Cycles per line
0	1/0	0	0	0	0	16 clocks
0	1/0	0	0	0	1	17 clocks
0	1/0	0	0	1	0	18 clocks
0	1/0	0	0	1	1	19 clocks
0	1/0	0	1	0	0	20 clocks
0	1/0	0	1	0	1	21 clocks
0	1/0	0	1	1	0	22 clocks
0	1/0	0	1	1	1	23 clocks
0	1/0	1	0	0	0	24 clocks
0	1/0	1	0	0	1	25 clocks
0	1/0	1	0	1	0	26 clocks
0	1/0	1	0	1	1	27 clocks
0	1/0	1	1	0	0	28 clocks
0	1/0	1	1	0	1	29 clocks
0	1/0	1	1	1	0	30 clocks
0	1/0	1	1	1	1	31 clocks
1	1	0	0	0	0	32 clocks
1	1	0	0	0	1	33 clocks
1	1	0	0	1	0	34 clocks
1	1	0	0	1	1	35 clocks
1	1	0	1	0	0	36 clocks
1	1	0	1	0	1	37 clocks
1	1	0	1	1	0	38 clocks
1	1	0	1	1	1	39 clocks
1	1	1	0	0	0	40 clocks
1	1	1	0	0	1	41 clocks
1	1	1	0	1	0	42 clocks
1	1	1	0	1	1	43 clocks
1	1	1	1	0	0	44 clocks
1	1	1	1	0	1	45 clocks
1	1	1	1	1	0	46 clocks
1	1	1	1	1	1	47 clocks
1	1	0	0	0	0	48 clocks
1	1	0	0	0	1	49 clocks
1	1	0	0	1	0	50 clocks
1	1	0	0	1	1	51 clocks
1	1	0	1	0	0	52 clocks

RTNE5	RTNE4	RTNE3	RTNE2	RTNE1	RTNE0	Clock Cycles per line
1	1	0	1	0	1	53 clocks
1	1	0	1	1	0	54 clocks
1	1	0	1	1	1	55 clocks
1	1	1	0	0	0	56 clocks
1	1	1	0	0	1	57 clocks
1	1	1	0	1	0	58 clocks
1	1	1	0	1	1	59 clocks
1	1	1	1	0	0	60 clocks
1	1	1	1	0	1	61 clocks
1	1	1	1	1	0	62 clocks
1	1	1	1	1	1	63 clocks

DIVE1-0: To specified the division ratio of internal operation clock frequency. Set the RTNE and DIVE bits to adjust Source line charge time. Be aware of that if the number of lines for driving liquid crystal is changed, the frame frequency must also be adjusted. Moreover, In system interface mode, the DIVE1-0 bits are disabled. **Table 5-34** summarized the function of DIVE1-0 setting.

Table 5-34

DIVE1	DIVE0	Division Ratio	Internal Operation Clock Frequency
0	0	4	fosc / 4
0	1	2	fosc / 2
1	0	4	fosc / 4
1	1	8	fosc / 8

fosc =Frequency of RC oscillation

5.2.41. Panel Interface Control 5 (R97h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	NOWE3	NOWE2	NOWE1	NOWE0	0	0	0	0	0	0	0	0

NOWE [3:0]: Set the adjacent gate driver output non-overlap period in RGB interface. **Table 5-35** summarized the function of NOWE3-0 setting.

Table 5-35

NOWE3	NOWE2	NOWE1	NOWE0	Gate output non-overlap period Internal Operation (reference clock: internal oscillator)
0	0	0	0	2 clocks
0	0	0	1	2 clocks
0	0	1	0	4 clocks
0	0	1	1	6 clocks
0	1	0	0	8 clocks
0	1	0	1	10 clocks
0	1	1	0	12 clocks
0	1	1	1	14 clocks
1	0	0	0	16 clocks
1	0	0	1	18 clocks
1	0	1	0	20 clocks
1	0	1	1	22 clocks
1	1	0	0	24 clocks
1	1	0	1	26clocks
1	1	1	0	28 clocks
1	1	1	1	30 clocks

5.2.42. Write Display Brightness Value (RB1h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0

This command is used to adjust the brightness value of the display.

DBV[7:0]: Set the adjacent brightness value of the display. In principle relationship is that the 00h value means the lowest brightness and FFh value means the highest brightness.

5.2.43. Read Display Brightness Value (RB2h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
R	1	0	0	0	0	0	0	0	0	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0

This command is used to return the brightness value of the display.

DBV [7:0] is reset when display is in sleep-in mode.

DBV [7:0] is '0' when bit BCTRL of "5.2.44 Write CTRL Display (B3h)" command is '0'.

DBV [7:0] is manual set brightness specified with "5.2.44 Write CTRL Display (B3h) command when bit BCTRL is '1'.

When bit BCTRL of "5.2.44 Write CTRL Display (B3h)" command is '1' and bit C1/C0 of "5.2.46 Write Content Adaptive Brightness Control (B5h)" are '0', DBV[7:0] output is the brightness value specified with "5.2.42 Write Display Brightness (B1h)" command.

5.2.44. Write CTRL Display Value (RB3h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	LED_ ON	BC_OUT_ INV	0	0	BCTRL	0	DD	BL	0	0

This command is used to control display brightness.

LED_ON: This bit is used to control LENON pin.

0 = Off

1 = On

BC_OUT_INV: This bit is used to control BC_OUT signal polarity.

0 = Off : Original polarity of BC_OUT signal.

1 = On : Inversed polarity of BC_OUT signal.

BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display and keyboard.

0 = Off (Brightness registers are 00h, DBV[7..0])

1 = On (Brightness registers are active, according to the other parameters.)

DD: Display Dimming Control:

DD = 0: Display Dimming is off

DD = 1: Display Dimming is on

BL: Backlight Control On/Off

0 = Off (Completely turn off backlight circuit. Control lines must be low.)

1 = On

Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 -> 1 or 1-> 0. When BL bit change from "On" to "Off", backlight is turned off without gradual dimming, even if dimming-on (DD=1) are selected.

5.2.45. Read CTRL Display Value (RB4h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
R	1	0	0	0	0	0	0	LED_ ON	BC_OUT_ INV	0	0	BCTRL	0	DD	BL	0	0

This command returns brightness control values, see chapter: “5.2.44 Write CTRL Display (B3h)”.

5.2.46. Write Content Adaptive Brightness Control Value (RB5h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C1	C0

This command is used to set parameters for image content based adaptive brightness control functionality. **Table 5-36** summarized the function of C1-0 setting.

Table 5-36

C1	C0	Function
0	0	Off
0	1	User Interface Image
1	0	Still Picture
1	1	Moving Image

5.2.47. Read Content Adaptive Brightness Control Value (RB6h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
R	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C1	C0

This command is used to read the settings for image content based adaptive brightness control functionality

5.2.48. Write CABC Minimum Brightness Value (RBEh)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0

This command is used to set the minimum brightness value of the display for CABC function.

In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.

5.2.49. Read CABC Minimum Brightness Value (RBFh)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
R	1	0	0	0	0	0	0	0	0	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0

This command returns the minimum brightness value of CABC function.

In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. CMB[7:0] is CABC minimum brightness specified with “5.2.48 Write CABC minimum brightness (BEh)” command.

6. GRAM

Table 6-1 GRAM address and display panel position (SS = “0”)

S/G pin		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	….	S709	S710	S711	S712	S713	S714	S715	S716	S717	S718	S719	S720
GS=0	GS=1	DB17-0			DB17-0			DB17-0			DB17-0			….	DB17-0			DB17-0			DB17-0			DB17-0		
G1	G320	“00000"H			“00001"H			“00002"H			"00003"H			….	"000EC"H			"000ED"H			"000EE"H			"000EF"H		
G2	G319	"00100"H			"00101"H			"00102"H			"00103"H			….	"001EC"H			"001ED"H			"001EE"H			"001EF"H		
G3	G318	"00200"H			"00201"H			"00202"H			"00203"H			….	"002EC"H			"002ED"H			"002EE"H			"002EF"H		
G4	G317	"00300"H			"00301"H			"00302"H			"00303"H			….	"003EC"H			"003ED"H			"003EE"H			"003EF"H		
G5	G316	"00400"H			"00401"H			"00402"H			"00403"H			….	"004EC"H			"004ED"H			"004EE"H			"004EF"H		
G6	G315	"00500"H			"00501"H			"00502"H			"00503"H			….	"005EC"H			"005ED"H			"005EE"H			"005EF"H		
G7	G314	"00600"H			"00601"H			"00602"H			"00603"H			….	"006EC"H			"06ED"H			"06EE"H			"06EF"H		
G8	G313	"00700"H			"00701"H			"00702"H			"00703"H			….	“007EC"H			“007ED"H			“007EE"H			“007EF"H		
G9	G312	“00800"H			“00801"H			“00802"H			“00803"H			….	“008EC"H			“008ED"H			“008EE"H			“008EF"H		
G10	G311	“00900"H			“00901"H			“00902"H			“00903"H			….	“009EC"H			“009ED"H			“009EE"H			“009EF"H		
G11	G310	“00E00"H			“00E01"H			“00E02"H			“00E03"H			….	“00EEC"H			“00EED"H			“00EEE"H			“00EEF"H		
G12	G309	“00B00"H			“00B01"H			“00B02"H			“00B03"H			….	“00BEC"H			“00BED"H			“00BEE"H			“00BEF"H		
G13	G308	“00C00"H			“00C01"H			“00C02"H			“00C03"H			….	“00CEC"H			“00CED"H			“00CEE"H			“00CEF"H		
G14	G307	“00D00"H			“00D01"H			“00D02"H			“00D03"H			….	“00DEC"H			“00DED"H			“00DEE"H			“00DEF"H		
G15	G306	“00E00"H			“00E01"H			“00E02"H			“00E03"H			….	“00EEC"H			“00EED"H			“00EEE"H			“00EEF"H		
G16	G305	“00F00"H			“00F01"H			“00F02"H			“00F03"H			….	“00FEC"H			“00FED"H			“00FEE"H			“00FEF"H		
G17	G304	“01000"H			“01001"H			“01002"H			“01003"H			….	“010EC"H			“010ED"H			“010EE"H			“010EF"H		
G18	G303	“01100"H			“01101"H			“01102"H			“01103"H			….	“011EC"H			“011ED"H			“011EE"H			“011EF"H		
G19	G302	“01200"H			“01201"H			“01202"H			“01203"H			….	“012EC"H			“012ED"H			“012EE"H			“012EF"H		
G20	G301	“01300"H			“01301"H			“01302"H			“01303"H			….	“013EC"H			“013ED"H			“013EE"H			“013EF"H		
:	:	:			:			:			:				:			:			:			:		
:	:	:			:			:			:				:			:			:			:		
G313	G8	“13800"H			“13801"H			“13802"H			“13803"H			….	“138EC"H			“138ED"H			“138EE"H			“138EF"H		
G314	G7	“13900"H			“13901"H			“13902"H			“13903"H			….	“139EC"H			“139ED"H			“139EE"H			“139EF"H		
G315	G6	“13A00"H			“13A01"H			“13A02"H			“13A03"H			….	“13AEC"H			“13AED"H			“13AEE"H			“13AEF"H		
G316	G5	“13B00"H			“13B01"H			“13B02"H			“13B03"H			….	“13BEC"H			“13BED"H			“13BEE"H			“13BEF"H		
G317	G4	“13C00"H			“13C01"H			“13C02"H			“13C03"H			….	“13CEC"H			“13CED"H			“13CEE"H			“13CEF"H		
G318	G3	“13D00"H			“13D01"H			“13D02"H			“13D03"H			….	“13DEC"H			“13DED"H			“13DEE"H			“13DEF"H		
G319	G2	“13E00"H			“13E01"H			“13E02"H			“13E03"H			….	“13EEC"H			“13EED"H			“13EEE"H			“13EEF"H		
G320	G1	“13F00"H			“13F01"H			“13F02"H			“13F03"H			….	“13FEC"H			“13FED"H			“13FEE"H			“13FEF"H		

Table 6-2 GRAM address and display panel position (SS = “1”)

S/G pin		S1	S2	S3	S4	S5	…	S7	S8	S9	S10	S11	S12	….	S709	S710	S711	S712	S713	S714	S715	S716	S717	S718	S719	S720
GS=0	GS=1	DB17-0			DB17-0			DB17-0			DB17-0			….	DB17-0			DB17-0			DB17-0			DB17-0		
G1	G320	“000EF”H			“000EE”H			“000ED”H			“000EC”H			….	“00003”H			“00002”H			“00001”H			“00000”H		
G2	G319	“001EF”H			“001EE”H			“001ED”H			“001EC”H			….	“00103”H			“00102”H			“00101”H			“00100”H		
G3	G318	“002EF”H			“002AE”H			“002ED”H			“002EC”H			….	“00203”H			“00202”H			“00201”H			“00200”H		
G4	G317	“003EF”H			“003EE”H			“003ED”H			“003EC”H			….	“00303”H			“00302”H			“00301”H			“00300”H		
G5	G316	“004EF”H			“004EE”H			“004ED”H			“004EC”H			….	“00403”H			“00402”H			“00401”H			“00400”H		
G6	G315	“005EF”H			“005EE”H			“005ED”H			“005EC”H			….	“00503”H			“00502”H			“00501”H			“00500”H		
G7	G314	“006EF”H			“006EE”H			“006ED”H			“006EC”H			….	“00603”H			“00602”H			“00601”H			“00600”H		
G8	G313	“007EF”H			“007EE”H			“007ED”H			“007EC”H			….	“00703”H			“00702”H			“00701”H			“00700”H		
G9	G312	“008EF”H			“008EE”H			“008ED”H			“008EC”H			….	“00803”H			“00802”H			“00801”H			“00800”H		
G10	G311	“009EF”H			“009EE”H			“009ED”H			“009EC”H			….	“00903”H			“00902”H			“00901”H			“00900”H		
G11	G310	“00AEF”H			“00AEE”H			“00AED”H			“00AEC”H			….	“00E03”H			“00A02”H			“00A01”H			“00A00”H		
G12	G309	“00BEF”H			“00BEE”H			“00BED”H			“00BEC”H			….	“00B03”H			“00B02”H			“00B01”H			“00B00”H		
G13	G308	“00CEF”H			“00CEE”H			“00CED”H			“00CEC”H			….	“00C03”H			“00C02”H			“00C01”H			“00C00”H		
G14	G307	“00DEF”H			“00DEE”H			“00DED”H			“00DEC”H			….	“00D03”H			“00D02”H			“00D01”H			“00D00”H		
G15	G306	“00EEF”H			“00EEE”H			“00EED”H			“00EEC”H			….	“00E03”H			“00E02”H			“00E01”H			“00E00”H		
G16	G305	“00FEF”H			“00FEE”H			“00FED”H			“00FEC”H			….	“00F03”H			“00F02”H			“00F01”H			“00F00”H		
G17	G304	“010EF”H			“010EE”H			“010ED”H			“010EC”H			….	“01003”H			“01002”H			“01001”H			“01000”H		
G18	G303	“011EF”H			“011EE”H			“011ED”H			“011EC”H			….	“01103”H			“01102”H			“01101”H			“01100”H		
G19	G302	“012EF”H			“012EE”H			“012ED”H			“012EC”H			….	“01203”H			“01202”H			“01201”H			“01200”H		
G20	G301	“013EF”H			“013EE”H			“013ED”H			“013EC”H			….	“01303”H			“01302”H			“01301”H			“01300”H		
:	:	:			:			:			:				:			:			:			:		
:	:	:			:			:			:				:			:			:			:		
G233	G8	“E8EF”H			“138EE”H			“138ED”H			“138EC”H			….	“13803”H			“13802”H			“13801”H			“13800”H		
G234	G7	“139EF”H			“139EE”H			“139ED”H			“139EC”H			….	“13903”H			“13902”H			“13901”H			“13900”H		
G235	G6	“13AEF”H			“13AEE”H			“13AED”H			“13AEC”H			….	“13A03”H			“13A02”H			“13A01”H			“13A00”H		
G236	G5	“13BEF”H			“13BEE”H			“13BED”H			“13BEC”H			….	“13B03”H			“13B02”H			“13B01”H			“13B00”H		
G237	G4	“13CEF”H			“13CEE”H			“13CED”H			“13CEC”H			….	“13C03”H			“13C02”H			“13C01”H			“13C00”H		
G238	G3	“13DEF”H			“13DEE”H			“13DED”H			“13DEC”H			….	“13D03”H			“13D02”H			“13D01”H			“13D00”H		
G239	G2	“13EEF”H			“13EEE”H			“13EED”H			“13EEC”H			….	“13E03”H			“13E02”H			“13E01”H			“13E00”H		
G240	G1	“13FEF”H			“13FEE”H			“13FED”H			“13FEC”H			….	“13F03”H			“13F02”H			“13F01”H			“13F00”H		

7. INTERFACES

The OTM3225C provides different interfaces to meet the diverse need of small/medium size LCD. Based on the application requirement, there are three different display modes which are most used in end product.

1. Still picture display
2. Moving picture display.
3. Re-writing still pictures while moving picture are display.

For above three different display requirements, OTM3225C provides different interfaces to meet the requirement.

1. System interface
2. External interface (RGB interface)
3. VSYNC interface

System interface is suitable for still picture display while RGB interface and VSYNC interface are suitable for moving picture display. Be aware that RGB or VSYNC interface still can used to display still picture and system interface can also display moving picture. **Table 7-1** summarized different interfaces for different display requirement.

Table 7-1

Display State	Operation Mode	RAM access Mode(RM)	Display operation Mode (DM1-0)
Still pictures	Internal clock	System interface (RM = 0)	Internal clock operation (DM1-0 = 00)
Moving pictures	RGB interface	RGB interface (RM = 1)	RGB interface (DM1-0 = 01)
Rewrite still picture area while displaying moving pictures.	RGB interface	System interface (RM = 0)	RGB interface (DM1-0 = 01)
Moving pictures	VSYNC interface	System interface (RM = 0)	VSYNC interface (DM1-0 = 10)
Low Speed moving picture	RGB interface	RGB interface (RM = 1)	Internal clock operation (DM1-0 = 00)

7.1. System Interface

The system interfaces of OTM3225C can support 8-bit, 9-bit, 16-bit, 18-bit 80-system Interface and Serial Peripheral Interface (SPI), which can be set by the IM3/2/1/0 pins. The system interface can set instructions and access RAM. **Table 7-2** summarized the interface corresponding to IM3-0 setting.

Table 7-2

IM3	IM2	IM1	IM0	MPU-Interface Mode	DB Pin in use
0	0	0	0	Setting disabled	-
0	0	0	1	Setting disabled	-
0	0	1	0	80-system 16-bit interface	DB17 to 10 and 8 to 1
0	0	1	1	80-system 8-bit interface	DB17 to 10
0	1	0	*/ID	Serial peripheral interface (SPI)	- (Note: SPI use SDI & SDO)
0	1	1	0	Setting disabled	-
1	0	0	0	Setting disabled	-
1	0	0	1	Setting disabled	-
1	0	1	0	80-system 18-bit interface	DB17 to 0
1	0	1	1	80-system 9-bit interface	DB17 to 9
1	1	*	*	Setting disabled -	-

7.1.1. 80-system 18-bit interface

The instruction and GRAM accessing format of 80-system 18-bit interface are shown in **Figure 7-1** and **Figure 7-2**, respectively.

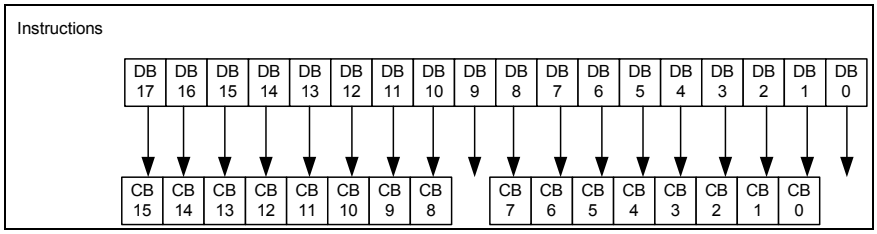


Figure 7-1

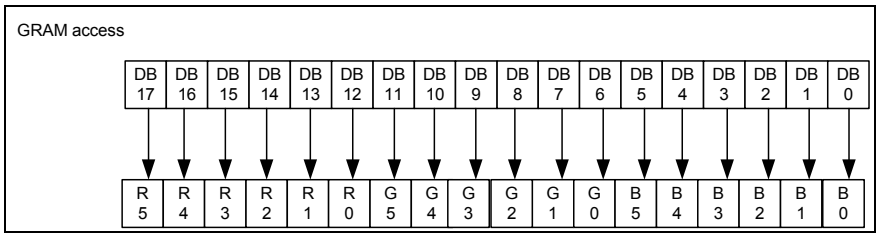


Figure 7-2

7.1.2. 80-system 16-bit interface

The instruction and GRAM accessing format of 80-system 16-bit interface are shown in **Figure 7-3** and **Figure 7-4**, respectively.

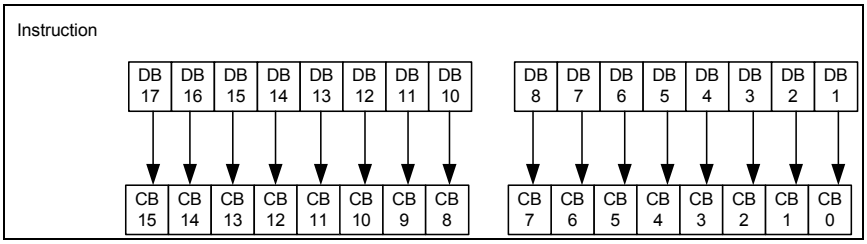


Figure 7-3

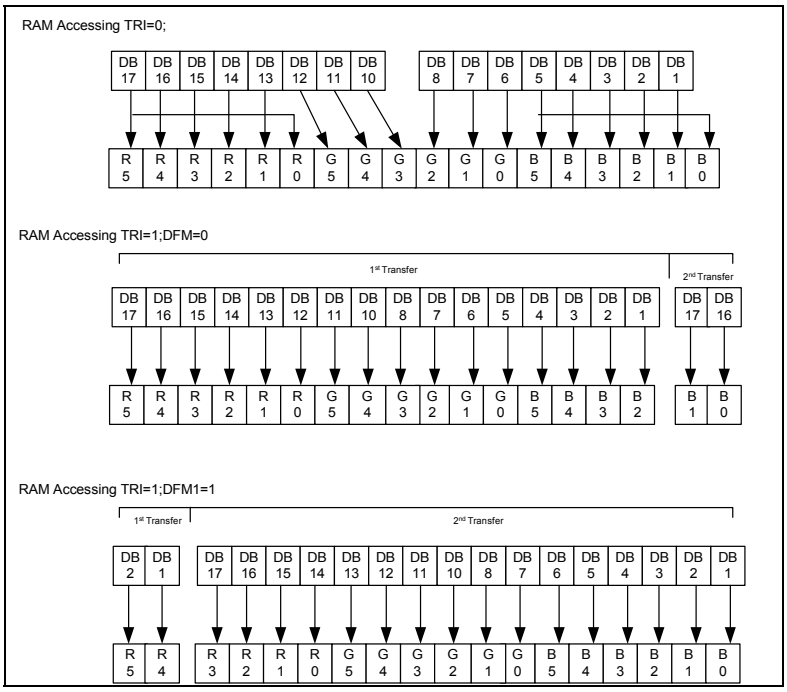


Figure 7-4

7.1.3. 80-system 9-bit interface

The instruction and GRAM accessing format of 80-system 9-bit interface are shown in **Figure 7-5** and **Figure 7-6**, respectively.

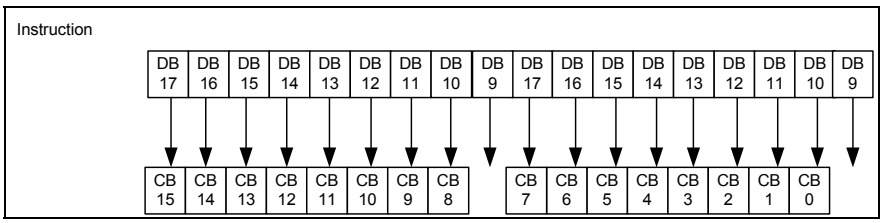


Figure 7-5

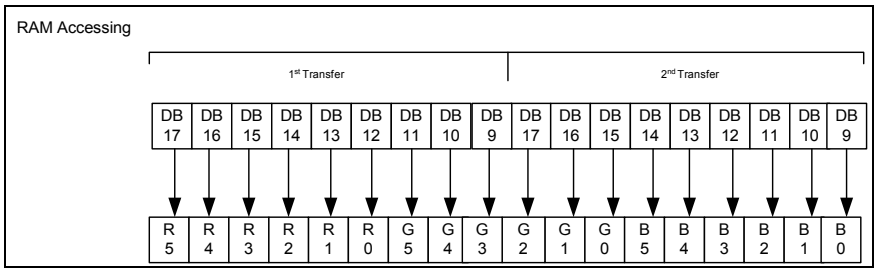


Figure 7-6

7.1.4. 80-system 8-bit interface

The instruction and GRAM accessing format of 80-system 8-bit interface are shown in **Figure 7-7** and **Figure 7-8**, respectively.

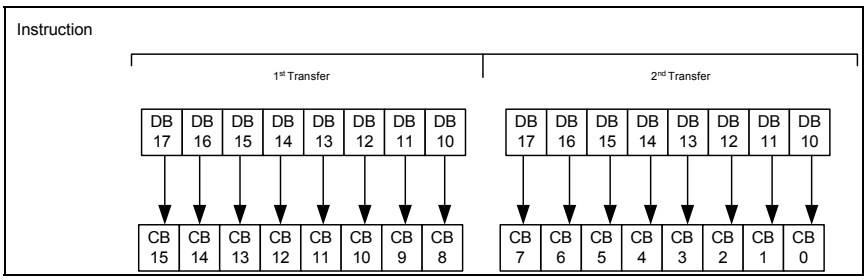


Figure 7-7

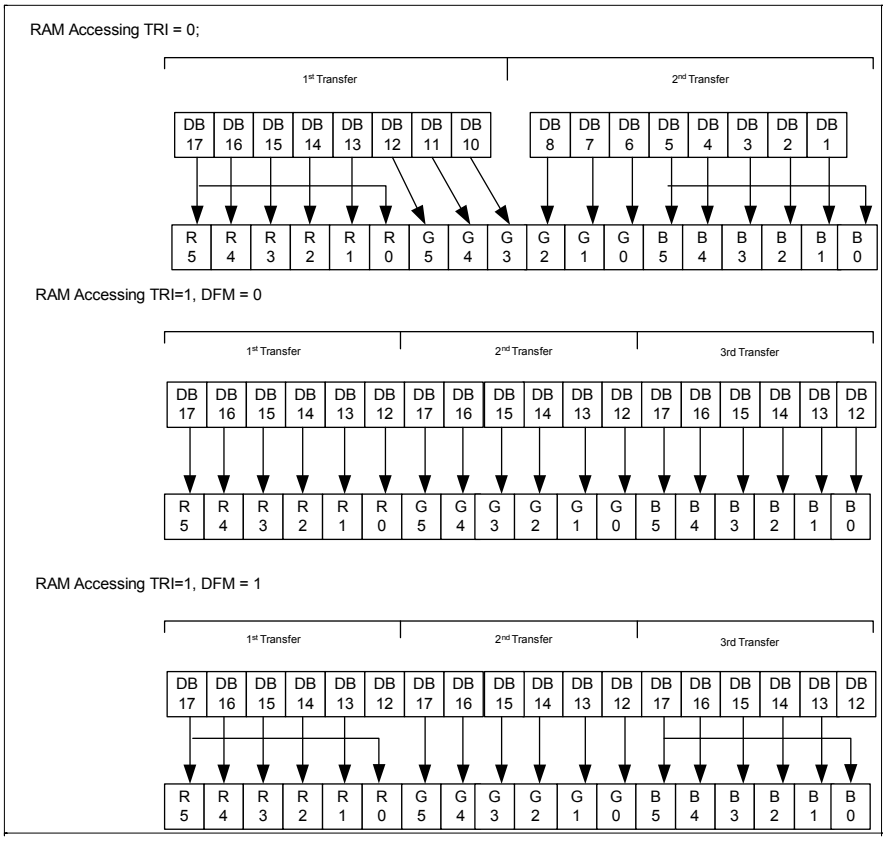


Figure 7-8

7.1.5. Serial Peripheral interface (SPI)

The system interface of OTM3225C also includes the Serial Peripheral Interface (SPI). In SPI mode, /CS, SCL, SDI and SDO are used to transfer data between MCU and OTM3225C. IM0/ID pin served as the ID pin. **Figure 7-9** illustrates the detail timing while using SPI. Be aware that the unused pins such as DB17-0 pins must be fixed at either IOVCC or GND level.

The instruction and GRAM accessing format of SPI interface are shown in **Figure 7-10** and **Figure 7-11**, respectively.
When read operation is desired In SPI mode, valid data are read out as the OTM3225C reads out the 6th byte data from the internal GRAM. The RAM data transfer in SPI mode, in SPI mode with status read are illustrated in **Figure 7-12**, , respectively.

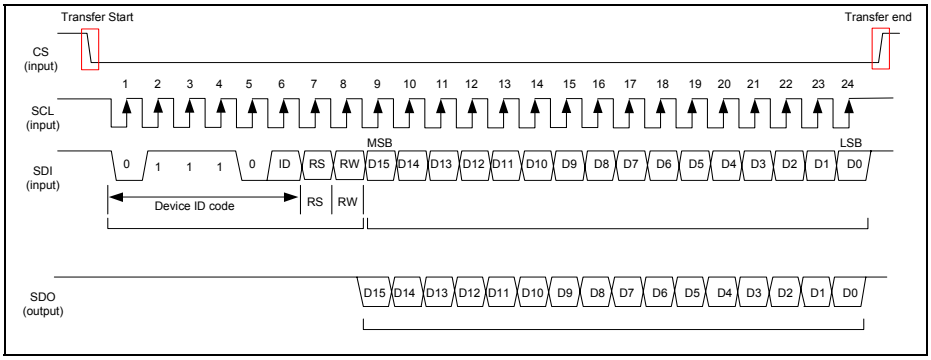


Figure 7-9

Start Byte Format

Transferred bits	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID		

Note 1) ID bit is selected by setting the IM0/ID pin.

RS	R/W	Function
0	0	Set an index register
0	1	Read a status
1	0	Write an instruction or RAM data
1	1	Read an instruction or RAM data

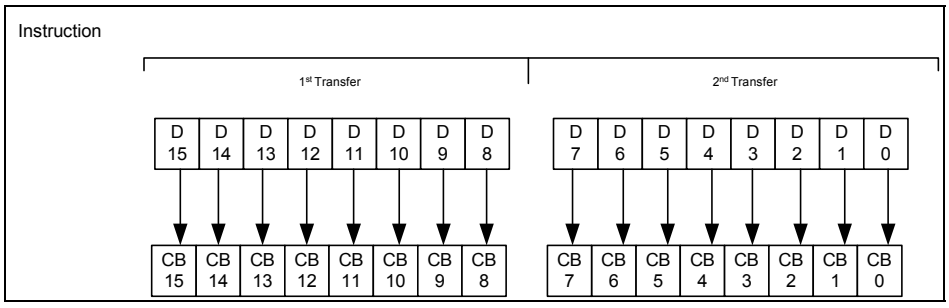


Figure 7-10

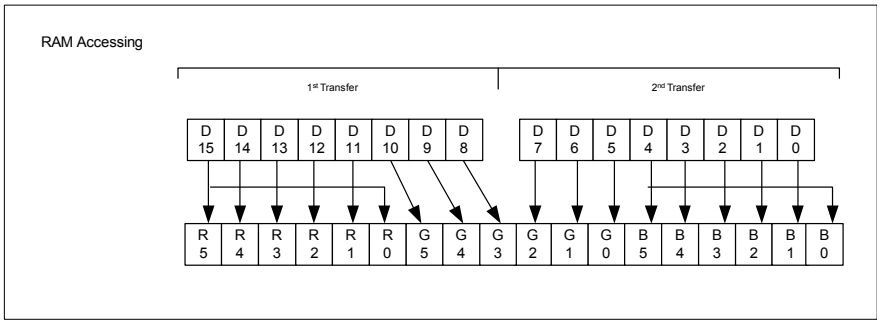


Figure 7-11

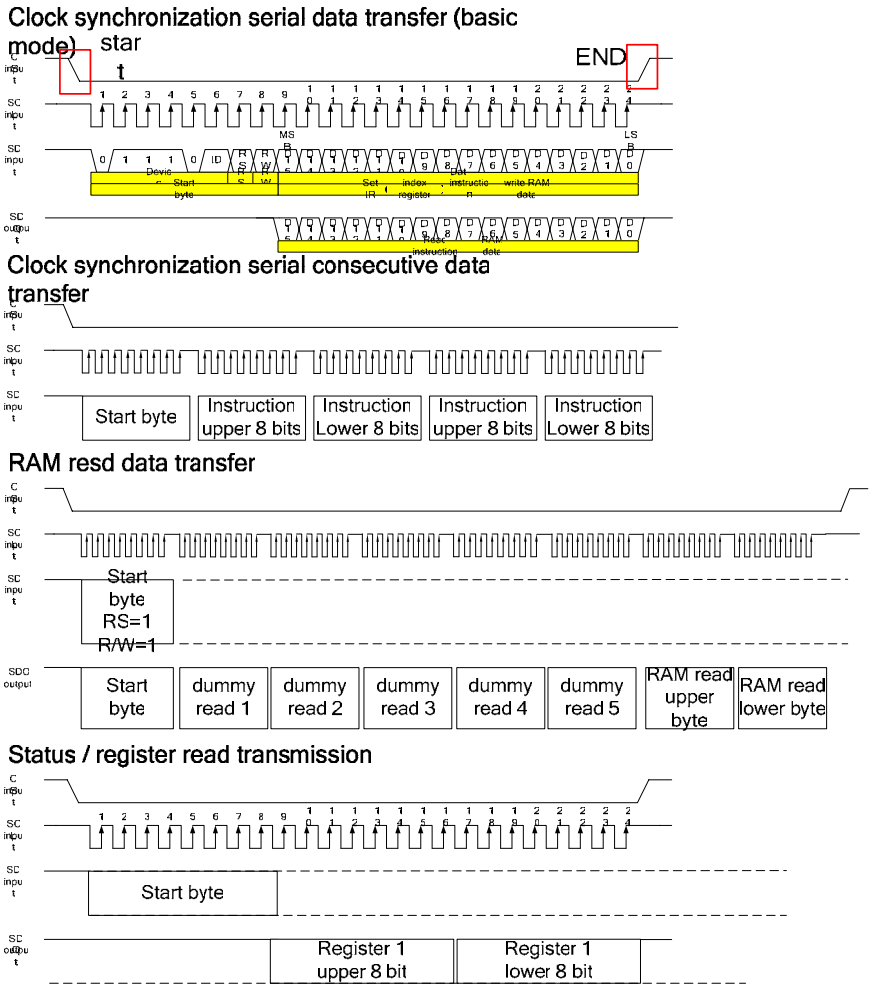


Figure 7-12

7.2. VSYNC Interface

The OTM3225C also supports VSYNC interface for moving picture display, which is the system interface in synchronization with the frame-synchronizing signal (VSYNC). The VSYNC interface can display a moving picture without tremendous modification.

DM1-0 = “10” and RM = “0” can initialized VSYNC interface. In VSYNC interface mode, the internal display operation is synchronized with the VSYNC signal. In VSYNC interface mode, the graphic data are stored in GRAM to minimize the data transfer to overwrite on the moving picture GRAM area. **Figure 7-13** illustrates moving picture data transfer through VSYNC interface.

In VSYNC mode, Internal operation is executed in synchronization with the internal clock generated from internal oscillators and VSYNC input. Therefore the frame rate is determined by the frequency of VSYNC. OTM3225C can access the internal RAM in high speed with less power consumption in VSYNC interface mode while using high-speed write mode

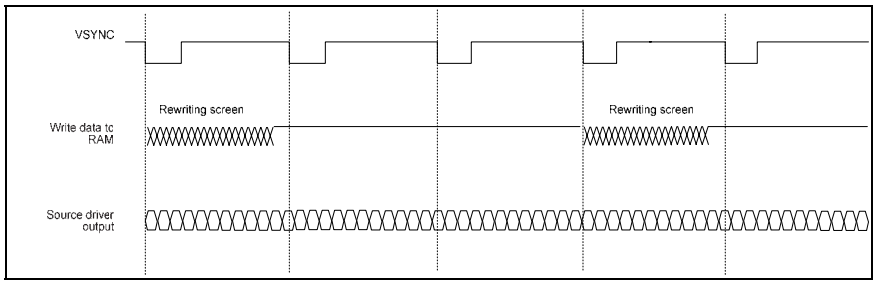


Figure 7-13

In VSYNC interface mode, the formula for Internal clock frequency and frame rate is shown below:

Input clock frequency = FrameRate x (DisplayLines) + FrontPorch + BackPorch x 16 x variance

Due to the possible cause of variances while set the internal clock frequency; be sure to complete the display operation in one VSYNC cycle.

7.3. External Display Interface

OTM3225C also includes external (RGB) interface for displaying moving picture. External interface can be set by RIM1-0 bit. **Table 7-3** summarized the corresponding types of RGB interface with RIM1-0 setting.

Table 7-3

RIM1	RIM0	RGB Interface	DB Pin
0	0	18-bit RGB interface	DB17-0
0	1	16-bit RGB interface	DB17-13, 11-1
1	0	6-bit RGB interface	DB17-12
1	1	8-bit RGB interface	DB17-10

RGB interface cab access OTM3225C by VSYNC, HSYNC, ENABLE, DOTCLK and DB17-0 signals, where VSYNC is used for frame synchronization; HSYNC is used for line synchronization and ENABLE is served as the valid data synchronized signals. The RGB interface can be rewriting minimum necessary data to the GRAM area which need to be overwritten with use of window address function and high-speed write mode. It is necessary for RGB interface to set front and back porch periods after and before a display period, respectively. **Figure 7-14** illustrates the general timing for RGB interface. There are some constrain while using RGB interface. The following summarized the conditions

(a) Partial display/ scroll function / interlace and graphics operation function are not available for RGB interface

(b) In RGB interface VSYNC, HSYNC, and DOTCLK signals must be input through a display operation period.

(c) The setting of the NO1-0 bits, STD1-0 bits and EQ1-0 bits are based on DOTCLK in RGB interface mode. In 6-bit RGB interface mode, it takes 3 DOTCLK inputs to transfer one pixel. Be aware data transfer in units of 3 DOTCLK inputs in 6-bit RGB interface mode is necessary. Set the cycle of each signal in 6-bit interface mode (VSYNC, HSYNC ENABLE, DB17-0) to input 3x clock to complete data transfer in units of pixels.

(d) In RGB interface mode, the front porch period continues until the next VSYNC input is detected after drawing one frame.

(e) In RGB interface mode, a GRAM address (DB17-0) is set in the address counter every frame on the falling edge of VSYNC.

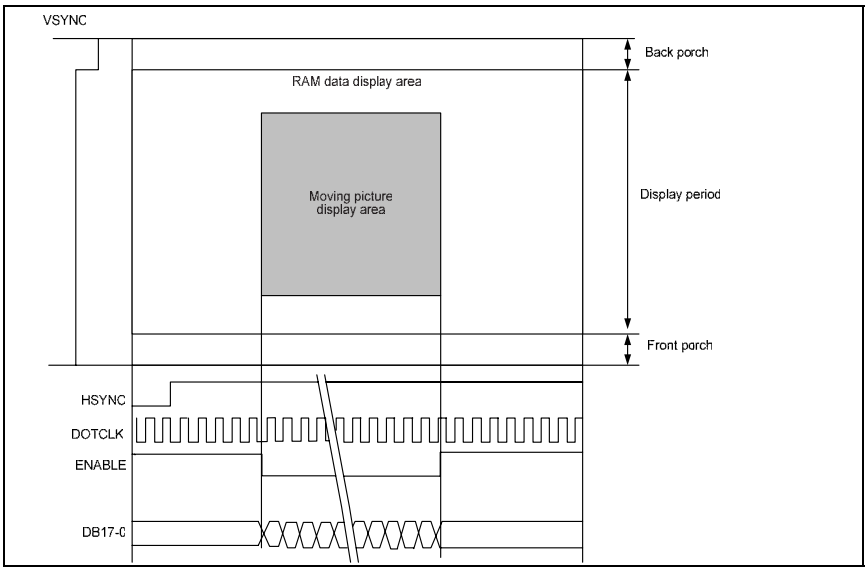


Figure 7-14

RGB interface includes ENABLE signal served as valid data synchronized signals. Moreover, the active level for ENABLE can be set by EPL. The EPL bit inverts the polarity of ENABLE signal. **Table 7-4** summarized the setting of EPL and ENABLE active level for GRAM accessing. Setting both EPL and ENABLE bits to automatically update RAM address in the AC is necessary while writing data to the GRAM.

Table 7-4

EPL	ENABLE	RAM Write	RAM Address
0	0	Enabled	Updated
0	1	Disabled	Retained
1	0	Disabled	Retained
1	1	Enabled	Updated

OTM3225C can support 18-bit, 16-bit , 8-bit and 6-bit RGB interface. The detail timing diagram for 18-bit, 16-bit and 6-bit RGB interface are shown in **Figure 7-15** and **Figure 7-16** respectively.

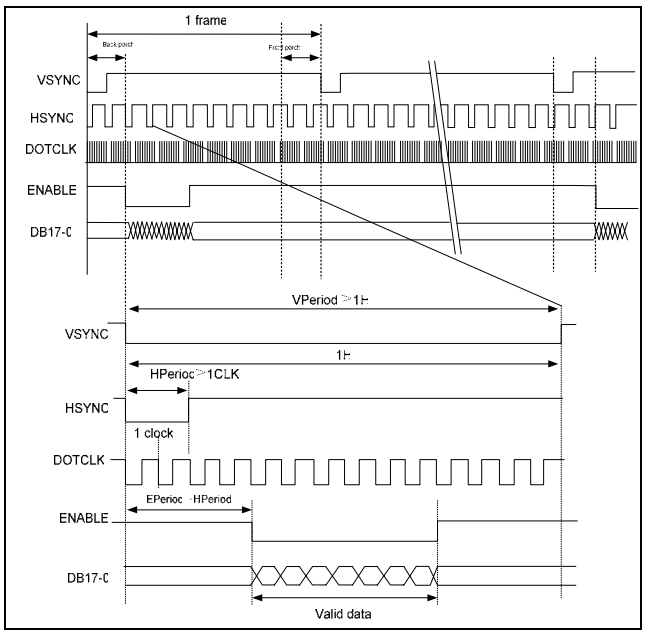


Figure 7-15

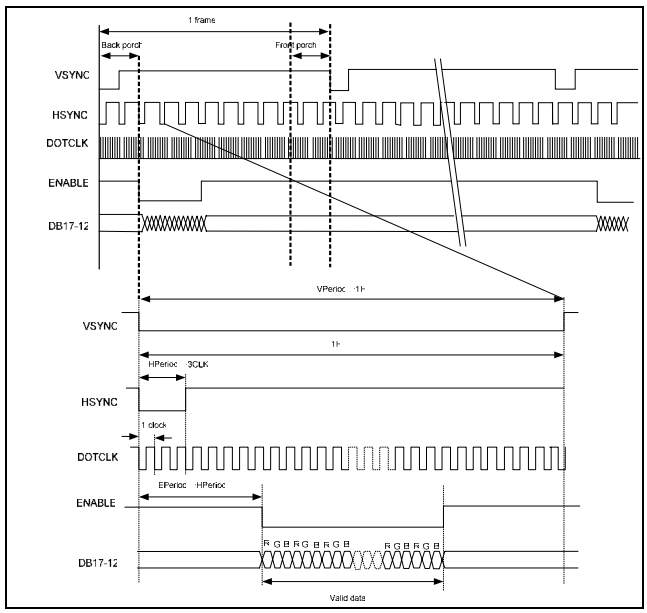


Figure 7-16

The RGB interface also has the window address function to transfer only minimum necessary data on the moving picture GRAM area, which can lower the power consumption and still can use system interface to rewrite data in still picture RAM area while displaying a moving picture. Setting RM = 0 while in RGB interface mode can make GRAM access through the system interface. When RGB interface accessing GRAM is desired, wait for one read/write bus cycle following by RM = 1 setting.

Figure 7-17 illustrates the timing diagram when displaying a moving picture through the RGB interface and rewriting data in the still picture GRAM area through the system interface.

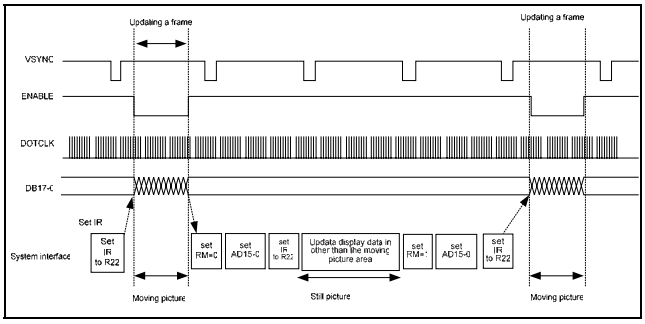


Figure 7-17

7.3.1. 6-bit RGB interface

RAM accessing format and data transmission synchronization of 6-bit RGB interface are shown in **Figure 7-18** and **Figure 7-19**, respectively.

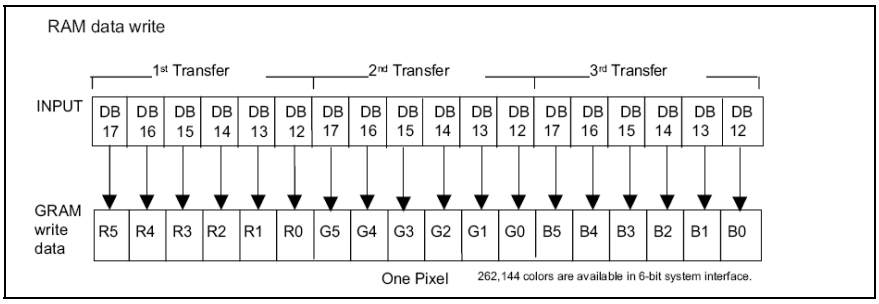


Figure 7-18

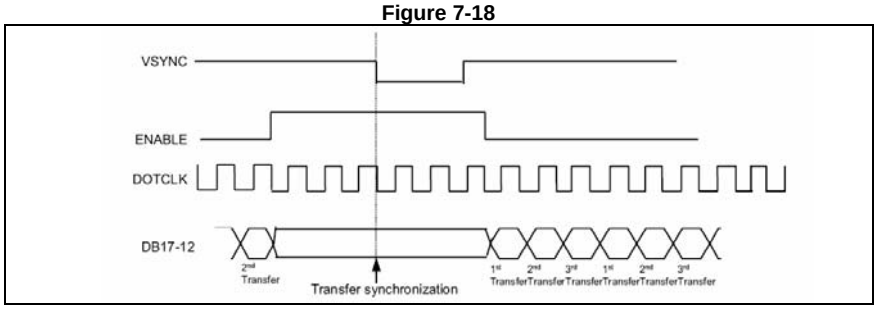


Figure 7-19

7.3.2. 16-bit RGB interface

RAM accessing format of 16-bit RGB interface are shown in **Figure 7-20**.

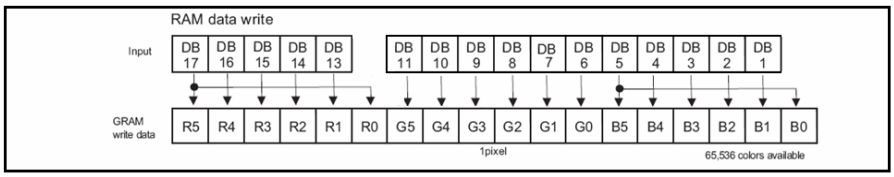


Figure 7-20

7.3.3. 18-bit RGB interface

RAM accessing format of 18-bit RGB interface are shown in **Figure 7-21**.

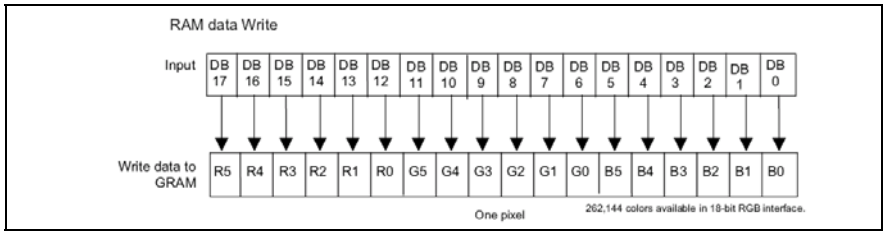
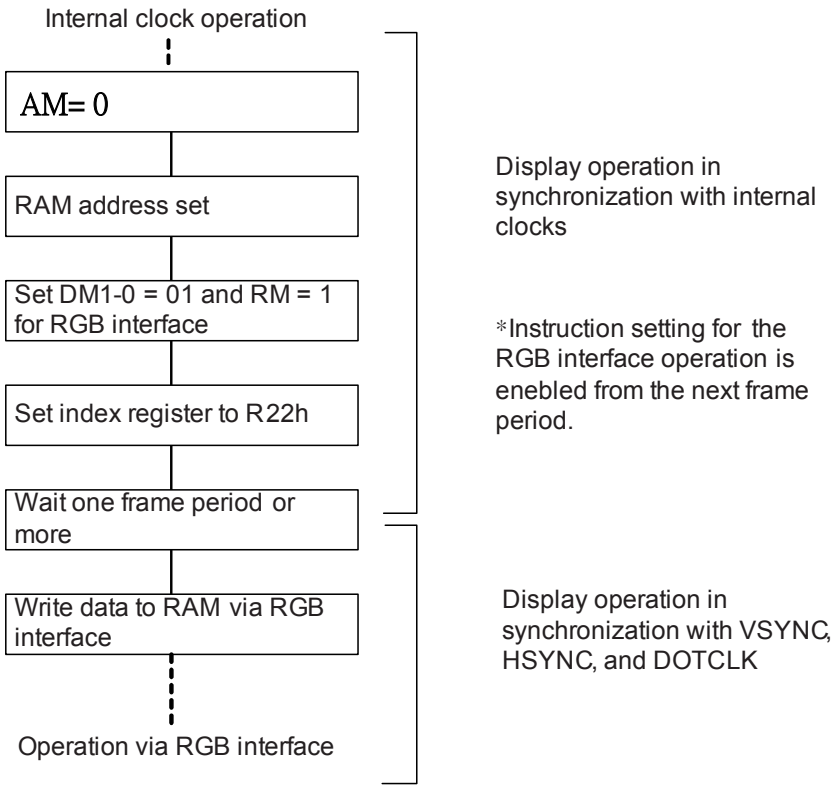


Figure 7-21

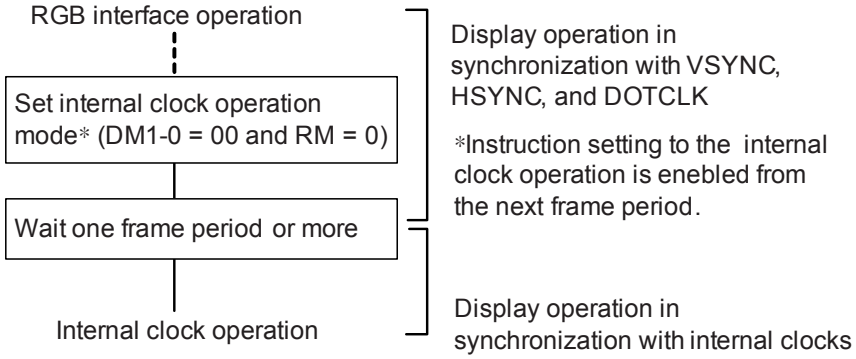
7.4. Sequence to set between system interface and RGB interface:

Internal Clock Operation to RGB Interface (1)



Note: Input the RGB interface signals before setting the DM 1-0 and RM bits to the RGB interface operation.

RGB Interface (1) to Internal Clock Operation



Note: Continue RGB interface signals at least for one frame period after setting DM1-0, RM bits to internal clock operation.

8. Display Feature Function:

8.1. FMARK function:

OTM3225C provided FMARK function which output signal to alert host MCU via FMARK I/O pad so that LCD display can avoid tearing effect. FMARK output position and interval can be set by FMP[8:0] and FMI[2:0], respectively.

Figure 8-1 illustrated the FMARK output position when FMP[8:0]=9'h008.

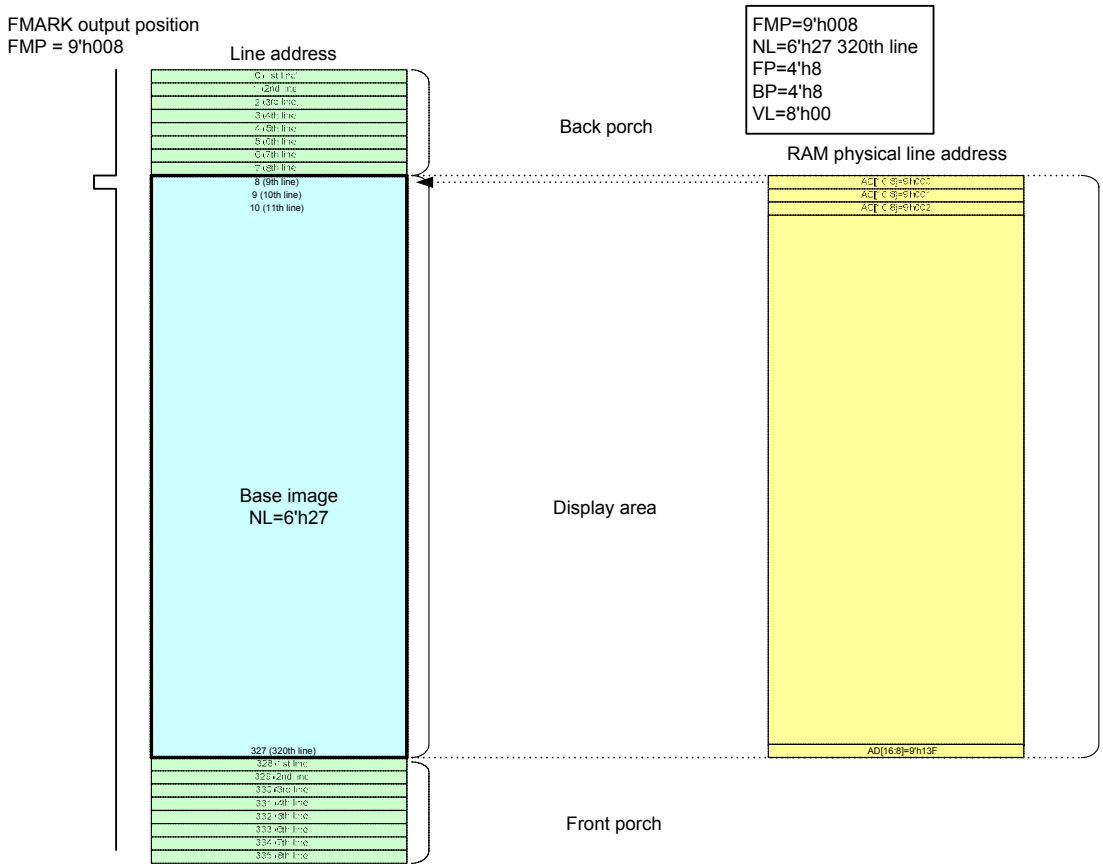
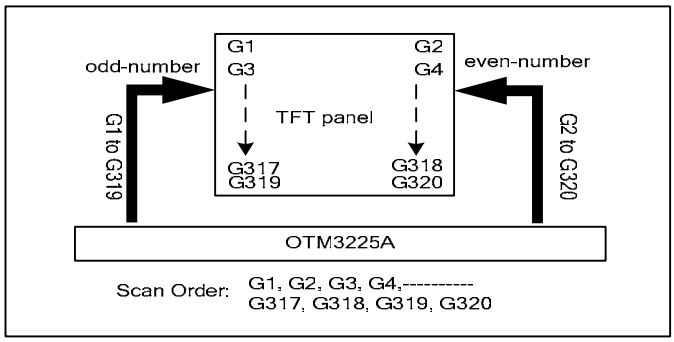
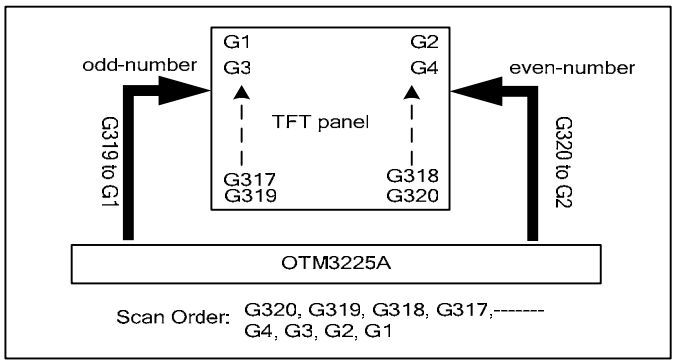
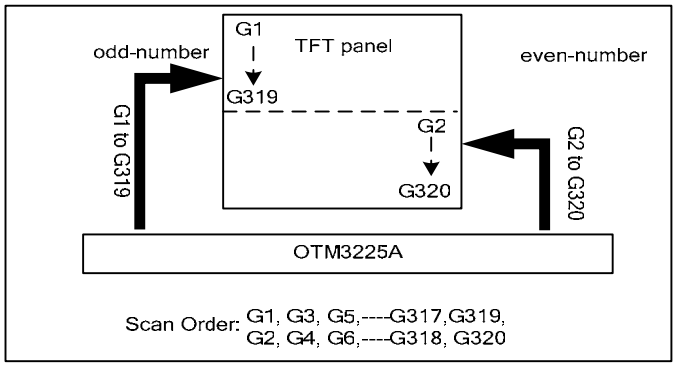
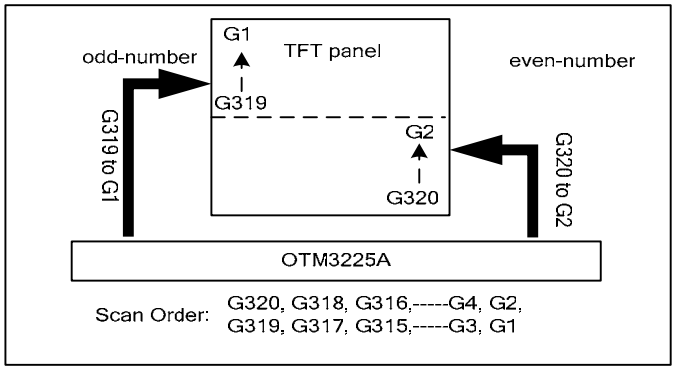


Figure 8-1 Example of FMARK signal.

8.2. Scan Mode function:

SM	GS	Scan Direction
0	0	
0	1	
1	0	
1	1	

8.3. Scaling function:

OTM3225C provides scaling function to resize the display area. The Scaling factor can be set via RSZ[1:0] (register R04h, CB [1:0]). Table summarized the RSZ[1:0] function. The image after scaling can be displayed at the area set by (HSA, HEA, VSA, VFA).

Table 8-1

RSZ[1:0]	Scaling Factor	Actual resolution (original input data 240xRGbx320)
00	No scaling	240xRGBx320
01	1/2 scaling	120xRGBx160
10	No scaling	240xRGBx320
11	1/4 scaling	60xRGBx80

Table 8-2 illustrated the data arrangement when scaling factor is 1/2, RSZ[1:0]='"01"

	1	2	3	4	5	6	7	8
1	A1	A2	A3	A4	A5	A6	A7	A8
2	B1	B2	B3	B4	B5	B6	B7	B8
3	C1	C2	C3	C4	C5	C6	C7	C8
4	D1	D2	D3	D4	D5	D6	D7	D8
5	E1	E2	E3	E4	E5	E6	E7	E8
6	F1	F2	F3	F4	F5	F6	F7	F8
7	G1	G2	G3	G4	G5	G6	G7	G8
8	H1	H1	H3	H4	H5	H6	H7	H8

	1	2	3	4
1	A1	A3	A5	A7
2	C1	C3	C5	C7
3	E1	E3	E5	E7
4	G1	G3	G5	G7

Table 8-3 data arrangement

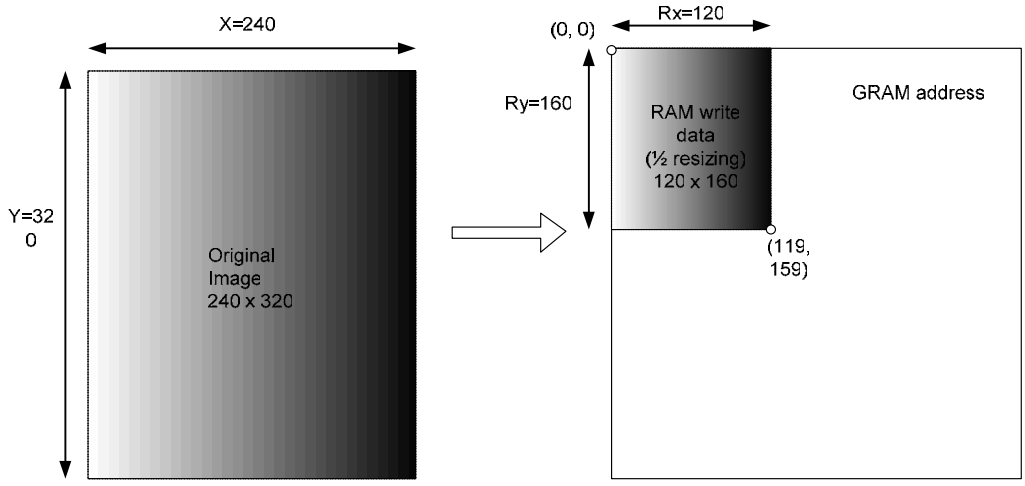
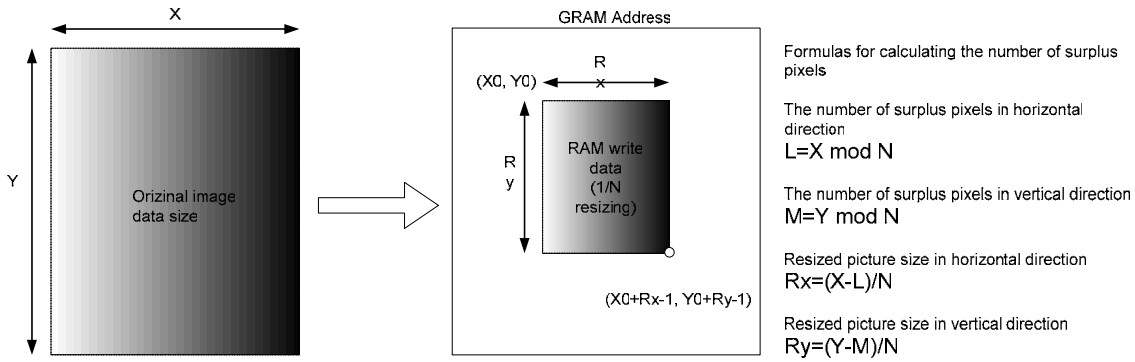
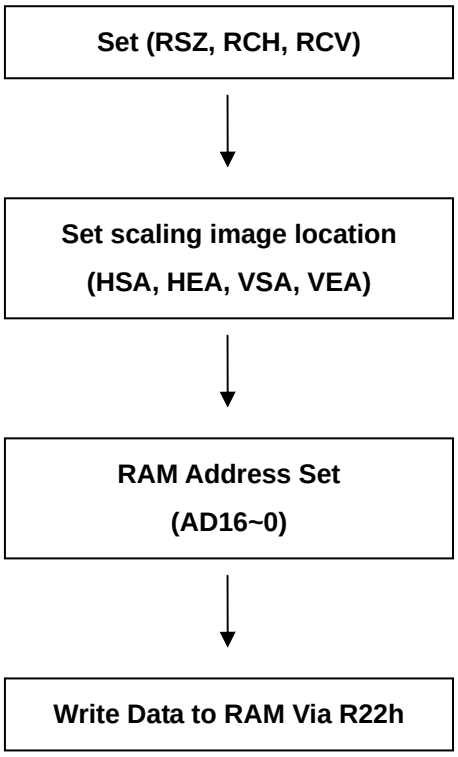


Figure 8-2 illustrated the example when scaling factor is 1/2, RSZ[1:0]='"01"



The flow chart to use scaling function:



8.4. Partial Display function:

OTM3225C has partial display function feature which can provide only partial display for power saving purpose. Partial display function can be accessed by setting BSEE="0",. Moreover, 2 partial display area (partial image 1/ partial image 2) can be initialized by set PTDE0="1" and PTDE1="1", respectively. The partial display area for partial image 1 and partial 2 can be set by PTSA0 / PTEA0 and PTSA1/ PTEA1, respectively. **Table 8-4** and **Figure 8-3** summarized the full and partial display function.

Table 8-4 Partial display function summary table

Case	Function Setting	Display area setting	Display Position
Full display	**BASEE="1"** **PTDE0="x"** **PTDE1="x"**	**(BSA,BEA)**	**-**
Partial image1:0n **Partial image2:Off**	**BASEE="0"** **PTDE0="1"** **PTDE1="0"**	**(PTSA0,PTEA0)**	**PTDP0**
Partial image1:Off **Partial image2:On**	**BASEE="0"** **PTDE0="0"** **PTDE1="1"**	**(PTSA1,PTEA1)**	**PTDP1**
Partail image1:On **Partial image2:On**	**BASEE="0"** **PTDE0="1"** **PTDE1="1"**	**(PTSA0,PTEA0)** **(PTSA1,PTEA1)**	**PTDP0 & PTDP1**

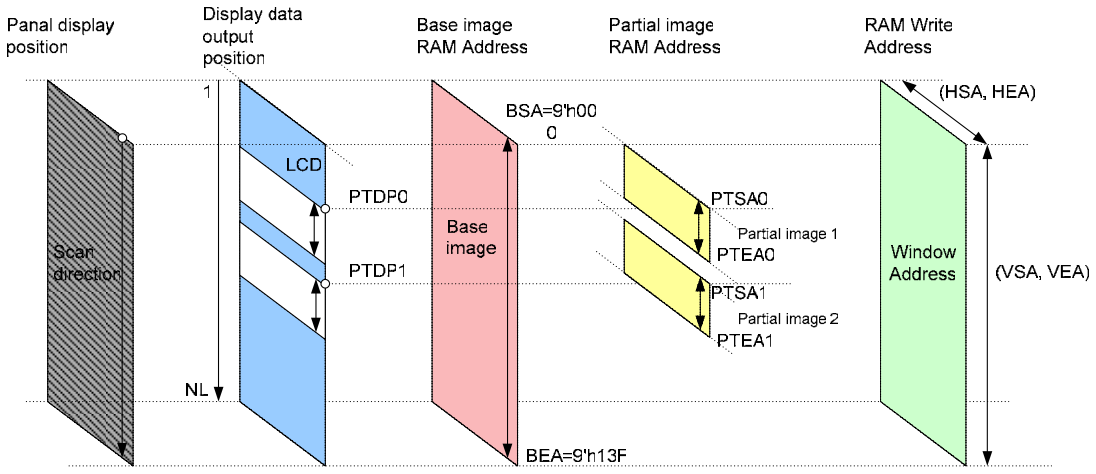


Figure 8-3 Partial display function diagram

Figure 8-4 indicated the case of NL[5:0] setting is < 6'h27 which active line is less than 320. Partial display image data can stored in not active area.

Figure 8-5 indicated the partial display area start position. The partial display area and start position can be set by (**PTSA0, PTEA0, PTSA1, PTEA1) and (PTDP0, PTDP1), respectively.**

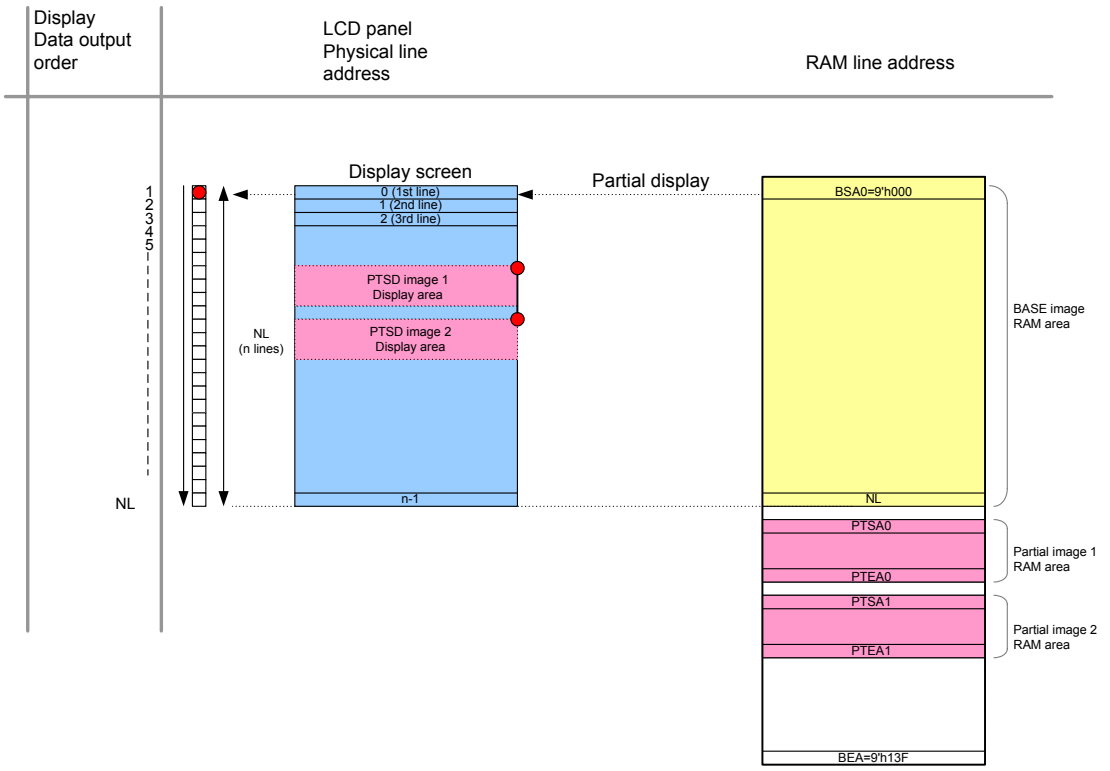


Figure 8-4 Example of NL[5:0] setting is < 6'h27 case

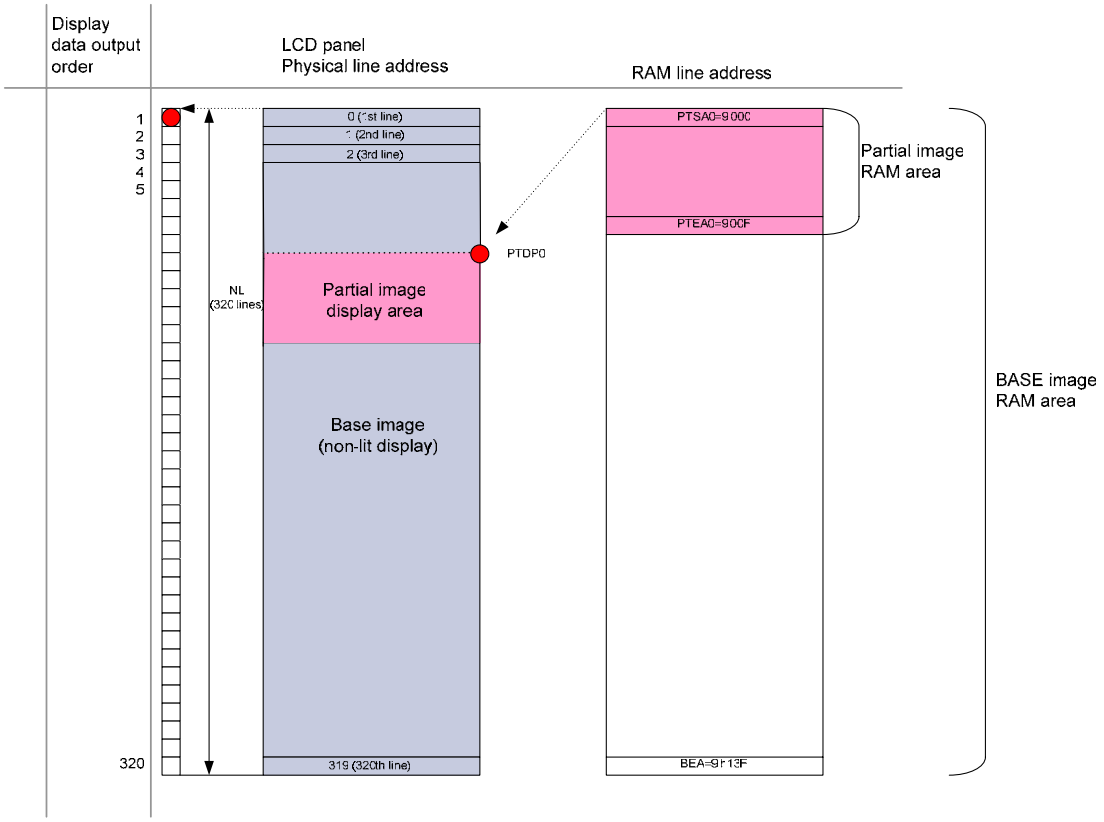


Figure 8-5 indicated the partial display area start position.

8.5. Gamma Correction functions:

	R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
R30	W	1	0	0	0	0	0	KP1[2]	KP1[1]	KP1[0]	0	0	0	0	0	KP0[2]	KP0[1]	KP0[0]
R31	W	1	0	0	0	0	0	KP3[2]	KP3[1]	KP3[0]	0	0	0	0	0	KP2[2]	KP2[1]	KP2[0]
R32	W	1	0	0	0	0	0	KP5[2]	KP5[1]	KP5[0]	0	0	0	0	0	KP4[2]	KP4[1]	KP4[0]
R35	W	1	0	0	0	0	0	RP1[2]	RP1[2]	RP1[0]	0	0	0	0	0	RP0[2]	RP0[2]	RP0[0]
R36	W	1	0	0	0	VRP1[4]	VRP1[3]	VRP1[2]	VRP1[1]	VRP1[0]	0	0	0	VRP0[4]	VRP0[3]	VRP0[2]	VRP0[1]	VRP0[0]
R37	W	1	0	0	0	0	0	KN1[2]	KN1[1]	KN1[0]	0	0	0	0	0	KN0[2]	KN0[1]	KN0[0]
R38	W	1	0	0	0	0	0	KN3[2]	KN3[1]	KN3[0]	0	0	0	0	0	KN2[2]	KN2[1]	KN2[0]
R39	W	1	0	0	0	0	0	KN5[2]	KN5[1]	KN5[0]	0	0	0	0	0	KN4[2]	KN4[1]	KN4[0]
R3C	W	1	0	0	0	0	0	RN1[2]	RN1[1]	RN1[0]	0	0	0	0	0	RN0[2]	RN0[1]	RN0[0]
R3D	W	1	0	0	0	VRN1[4]	VRN1[3]	VRN1[2]	VRN1[1]	VRN1[0]	0	0	0	VRN0[4]	VRN0[3]	VRN0[2]	VRN0[1]	VRN0[0]

γ **Control (R30h to R3Dh):** OTM3225C provides 10 gamma registers to fine tune gamma output voltage.

KP5-0[2:0]: γ **fine tune** registers for positive polarity.

RP1-0[2:0]: γ **gradient** registers for positive polarity.

VRP1-0[4:0]: γ **amplitude** registers for positive polarity.

KN5-0[2:0]: γ **fine tune** registers for positive polarity.

RN1-0[2:0]: γ **gradient** registers for positive polarity.

VRN1-0[4:0]: γ **amplitude** registers for positive polarity.

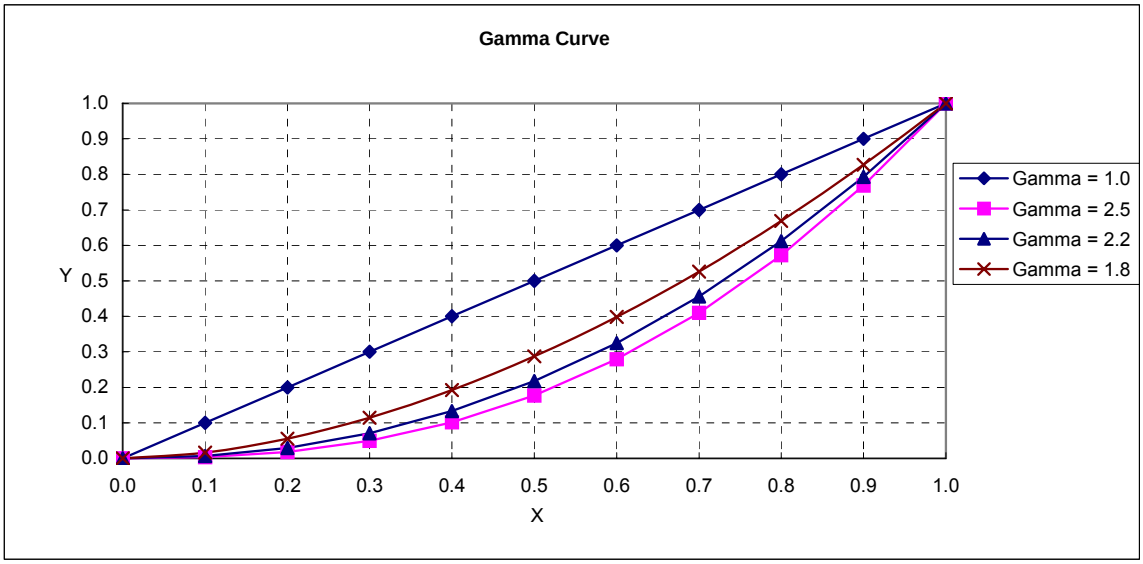
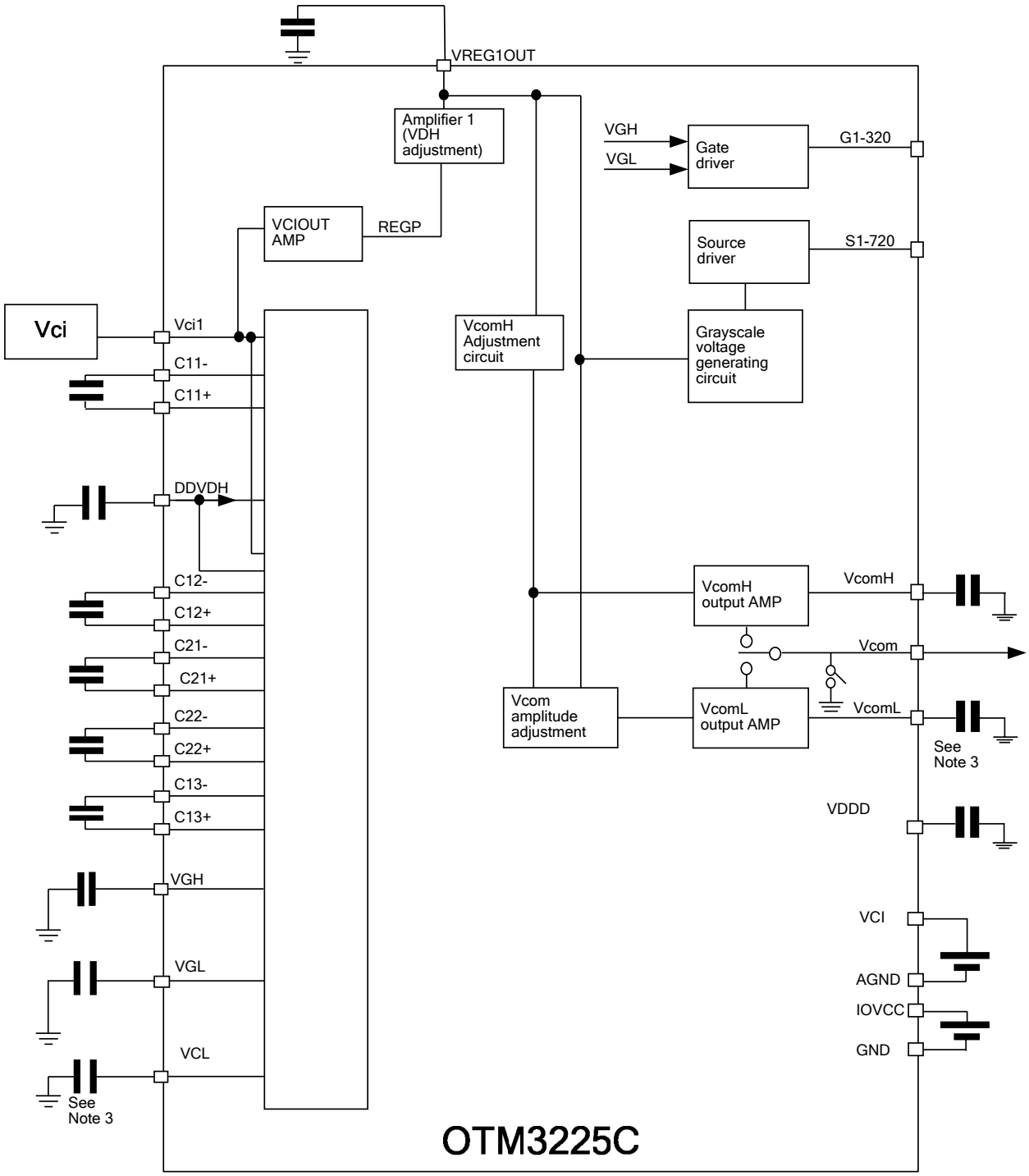


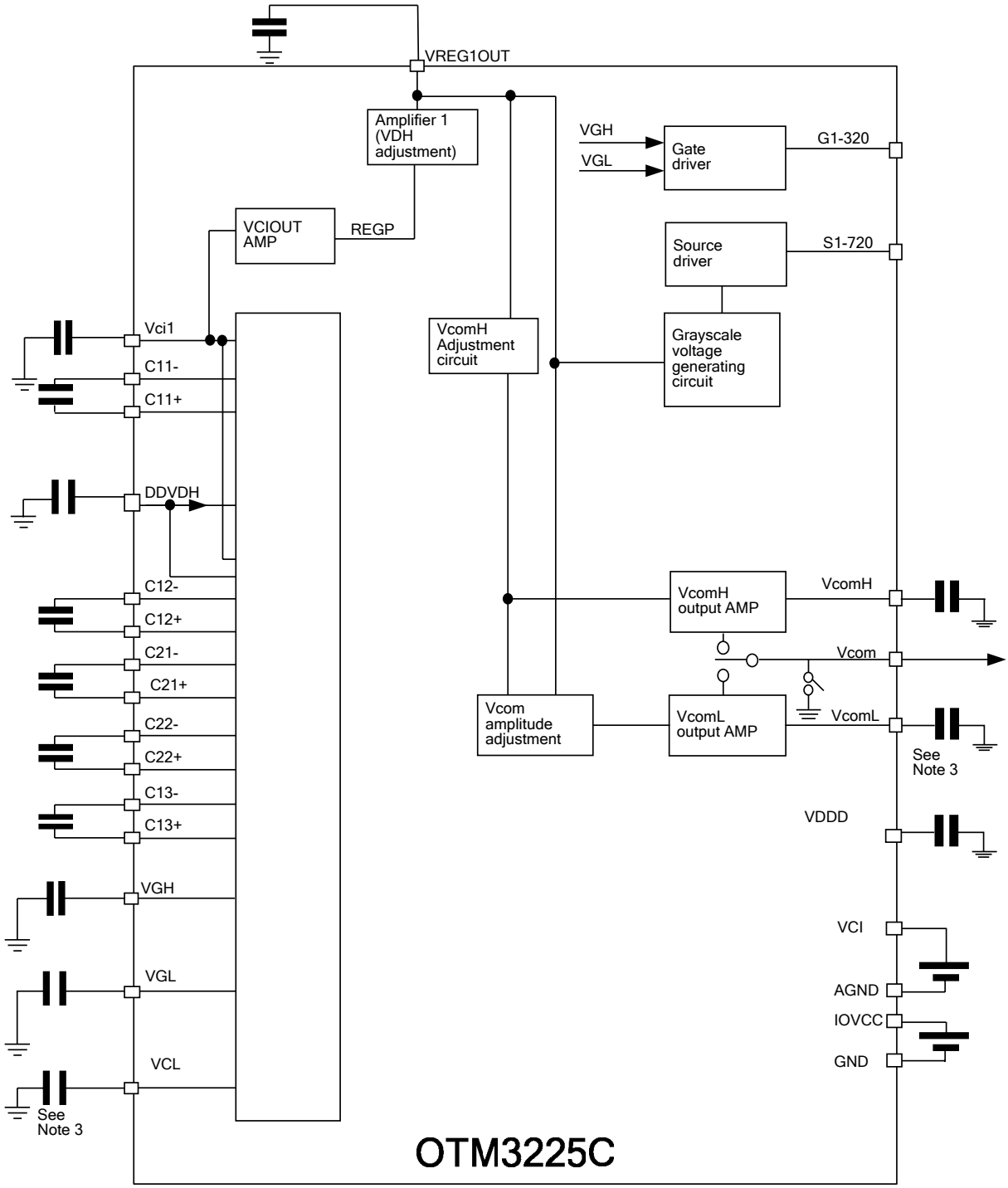
Figure 8-6 Illustrated 4 different Gamma Curve.

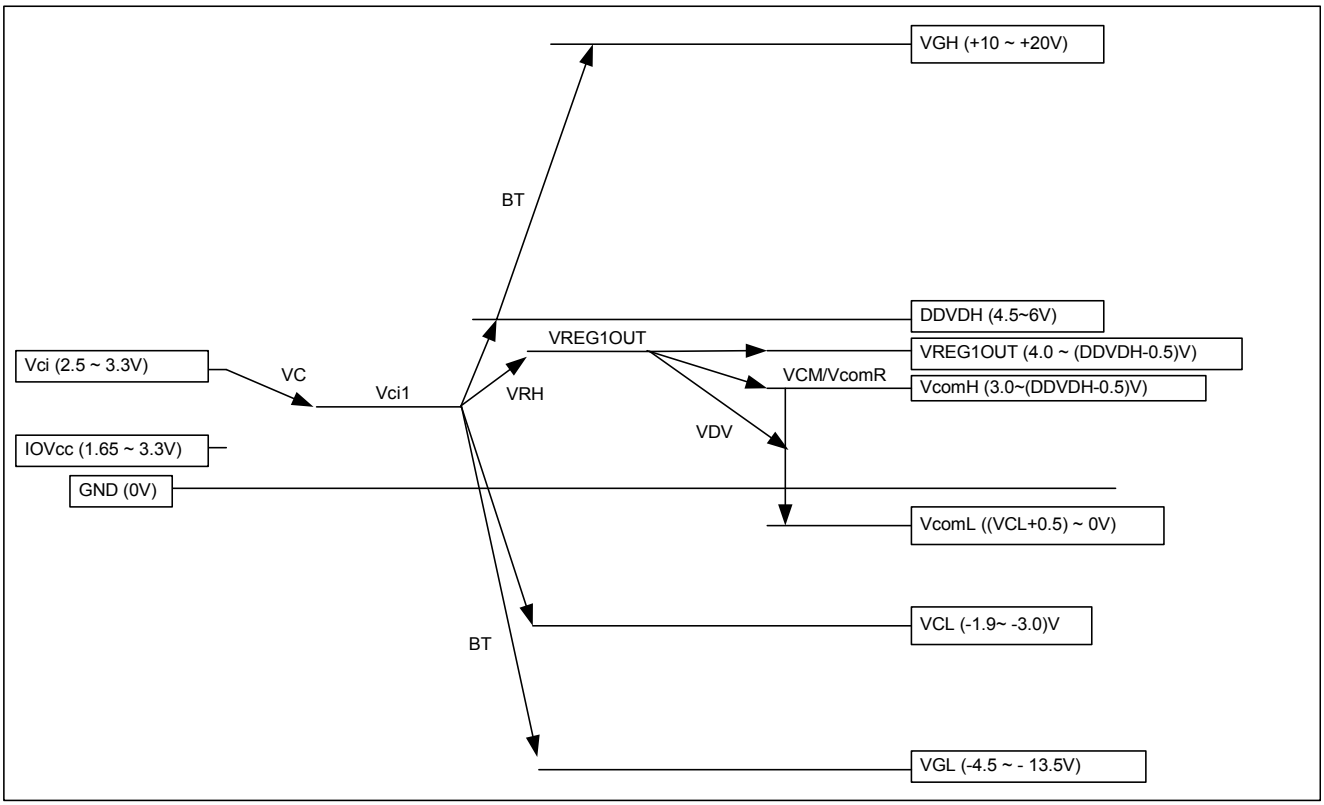
9. Power Management System:

(a) VCI short VCI1:

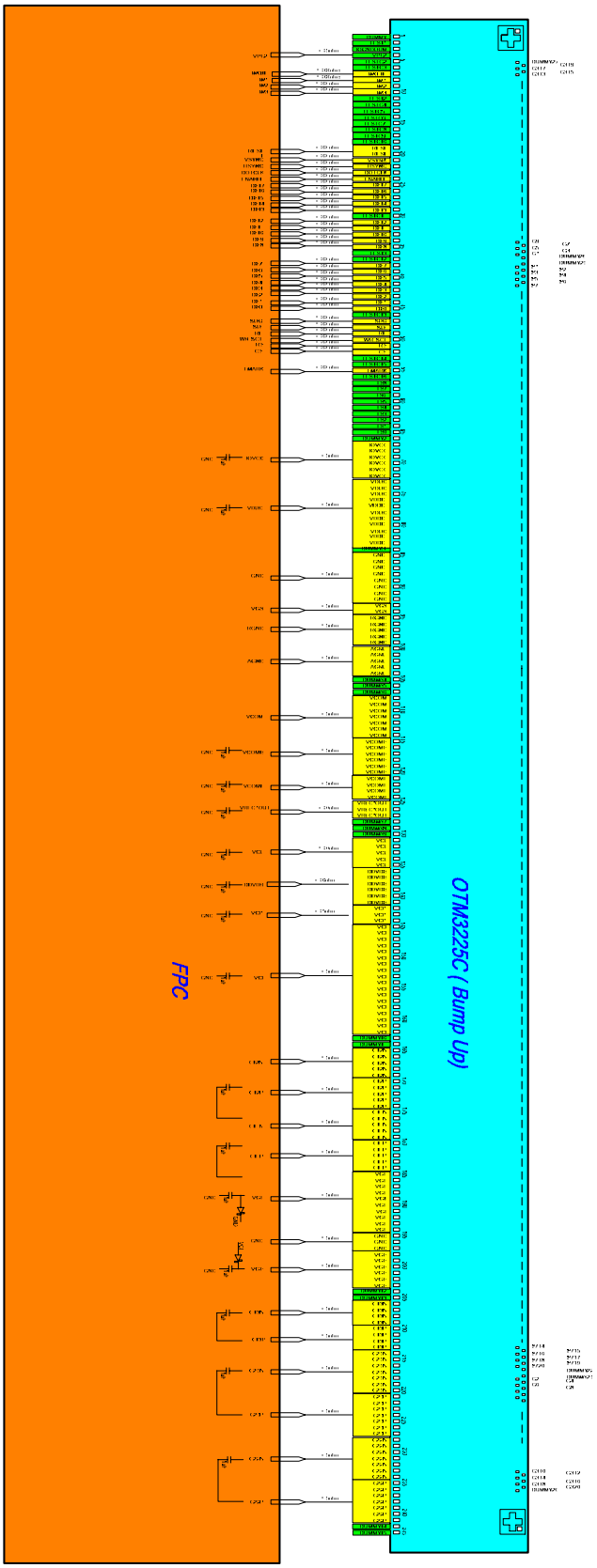


(b) Separate VCI and VCI1:




VGH (+10 ~ +20V)
BT
DDVDH (4.5~6V)
VREG1OUT
VREG1OUT (4.0 ~ (DDVDH-0.5)V)
Vci (2.5 ~ 3.3V)
VC
Vci1
VRH
VCM/VcomR
VcomH (3.0~(DDVDH-0.5)V)
VDV
IOVcc (1.65 ~ 3.3V)
GND (0V)
VcomL ((VCL+0.5) ~ 0V)
VCL (-1.9~ -3.0)V
BT
VGL (-4.5 ~ - 13.5V)

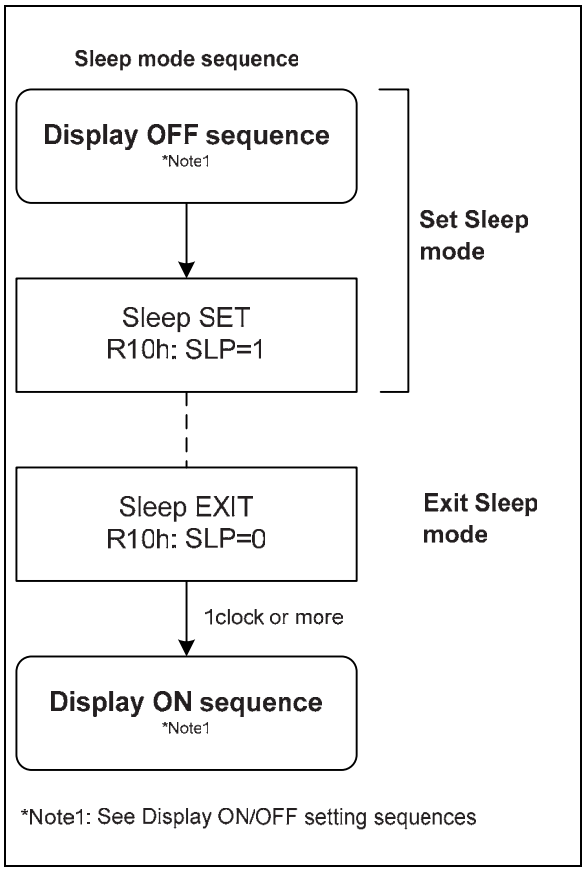
10. Application circuits:



11. Initial Code:

This initial code is not including Gamma setting. Please contact Orise Technology for desired Gamma setting.

11.1. Sequence to exit sleep mode:



12. Electrical Characteristics:

12.1. Absolute Maximum Ratings:

Table 12-1

Item	Symbol	Unit	Value	Note
Power Supply Voltage1	IOVCC – GND	V	-0.3 ～+4.6	
Power Supply Voltage 2	VCI – AGND	V	-0.3 ～+4.6	
Power Supply Voltage 3	DDVDH – AGND	V	-0.3 ～+6.5	
Power Supply Voltage4	AGND – VCL	V	-0.3 ～+4.6	
Power Supply Voltage 5	DDVDH – VCL	V	-0.3 ～+9.0	C, +11
Power Supply Voltage7	AGND – VGL	V	-0.3 ～+14.0	C, +16.5
Power Supply Voltage 8	VGH– VGL	V	-0.3 ～+30.0	
Input Voltage	Vt	V	-0.3 ～IOVCC + 0.3	
Operating Temperature	Topr	℃	-40 ～+85	
Storage Temperature	Tstg	℃	-55 ～+110	

12.2. DC Characteristics

Table 12-2 VCI= 2.50V～3.30V, IOVCC=1.65V～ 3.30V, Ta=-40℃～+85℃

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input High level voltage	VIH	V	IOVCC=1.65V～3.30V	0.8xIOVCC	-	IOVCC	
Input Low level voltage	VIL	V	IOVCC=1.65V～3.30V	-0.3	-	0.2xIOVCC	
Output "High" level voltage 1 (DB0-17)	VOH	V	IOVCC=1.65V～3.30V, IOH=-0.1mA	0.8xIOVCC	-	-	
Output "Low" level voltage 1 (DB0-17)	VOL	V	IOVCC=1.65V～3.30V, IOL=0.1mA	-	-	0.2xIOVCC	
I/O leak current	ILI	μA	Vin=0～IOVCC	-1	-	1	

12.3. AC Characteristics

VCI= 2.50V ~ 3.30V，IOVCC=1.65V ~ 3.30V，Ta=-40℃ ~ +85℃

12.3.1. Clock Characteristics

Table 12-3

Item	Symbol	Unit	Timing Diagram	Min.	Typ.	Max.	Note
RC Oscillation clock	fosc	kHz	IOVCC = VCI = 3.0V, 25°C		TBD		9

12.3.2. 80-System Bus Interface Timing Characteristics (18-/ 16- bit interface)

Table 12-4 Normal write operation, IOVCC=1.65V~3.30V

Item	Symbol		Unit	Min.	Typ.	Max.
Bus cycle time	Write	tCYCW	ns	125	-	-
	Read	tCYCR	ns	450	-	-
Write low-level pulse width		PWLW	ns	45	-	-
Read low-level pulse width		PWLR	ns	170	-	-
Write high-level pulse width		PWHW	ns	70	-	-
Read high-level pulse width		PWHR	ns	250	-	-
Write/Read rise/ fall time		tWRr, WRf	ns	-	-	25
Setup time	Write (RS to CS*,WR*)	tAS	ns	0	-	-
	Read (RS to CS*, RD*)		ns	10	-	-
Address Hold Time		tAH	ns	2	-	-
Write data setup time		tDSW	ns	25	-	-
Write data hold time		tH	ns	10	-	-
Read data delay time		tDDR	ns	-	-	150
Read data hold time		tDHR	ns	5	-	-

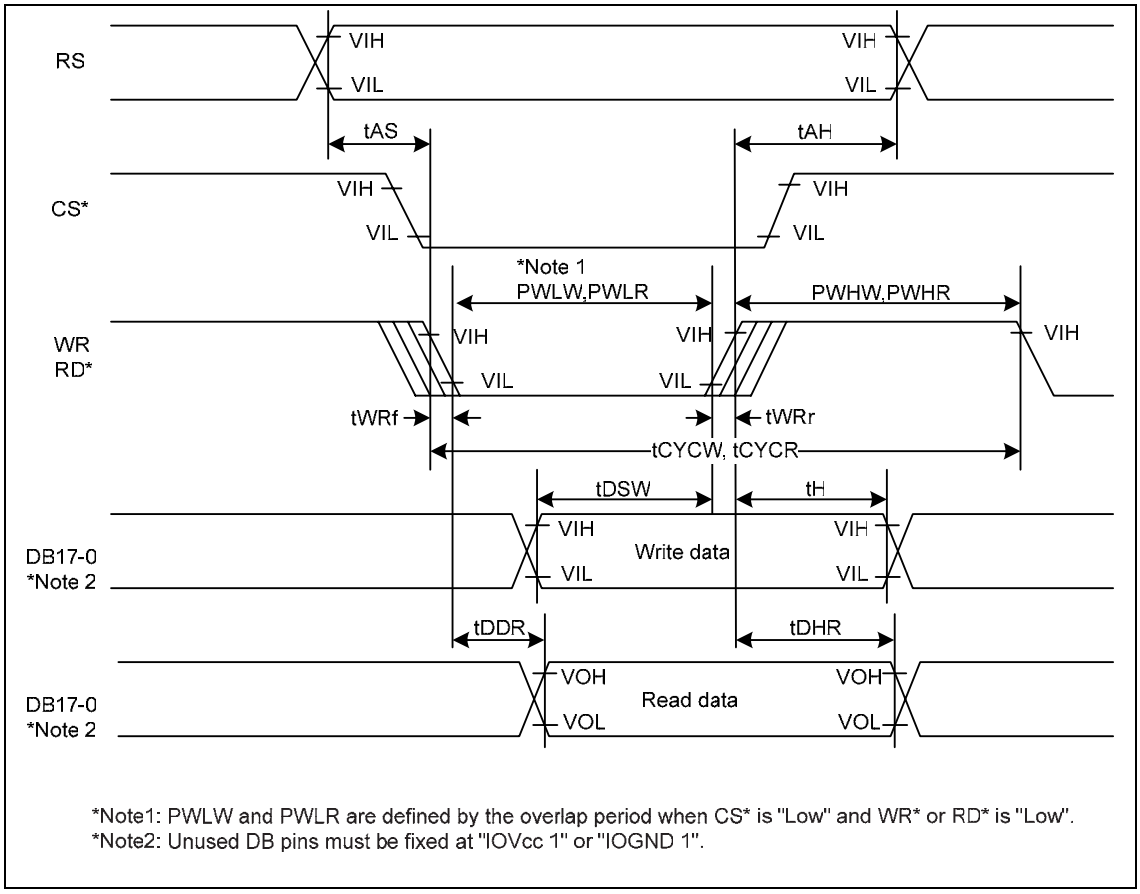


Figure 12-1 80-System Bus Interface

12.3.3. Clock-synchronized Serial Interface Timing Characteristics

Normal Write operation (IOVCC=1.65~3.30V)

Table 12-5

Item	Symbol		Unit	Min.	Typ.	Max.
Serial Time Clock Cycle	Write (received)	tSCYC	ns	100	-	20.000
	Read (transmitted)	tSCYC	ns	350	-	20.000
Serial Clock high-level width	Write (received)	tSCH	ns	40	-	-
	Read (transmitted)	tSCH	ns	150	-	-
Serial Clock low-level width	Write (received)	tSCL	ns	40	-	-
	Read (transmitted)	tSCL	ns	150	-	-
Serial clock rise/fall time		tSCr, tSCf	ns	-	-	20
Chip select setup time		tCSU	ns	20	-	-
Chip select hold time		tCH	ns	60	-	-
Serial input data setup time		tSISU	ns	30	-	-
Serial input data hold time		tSIH	ns	30	-	-
Serial output data delay time		tSOD	ns	-	-	130
Serial output data hold time		tSOH	ns	5	-	-

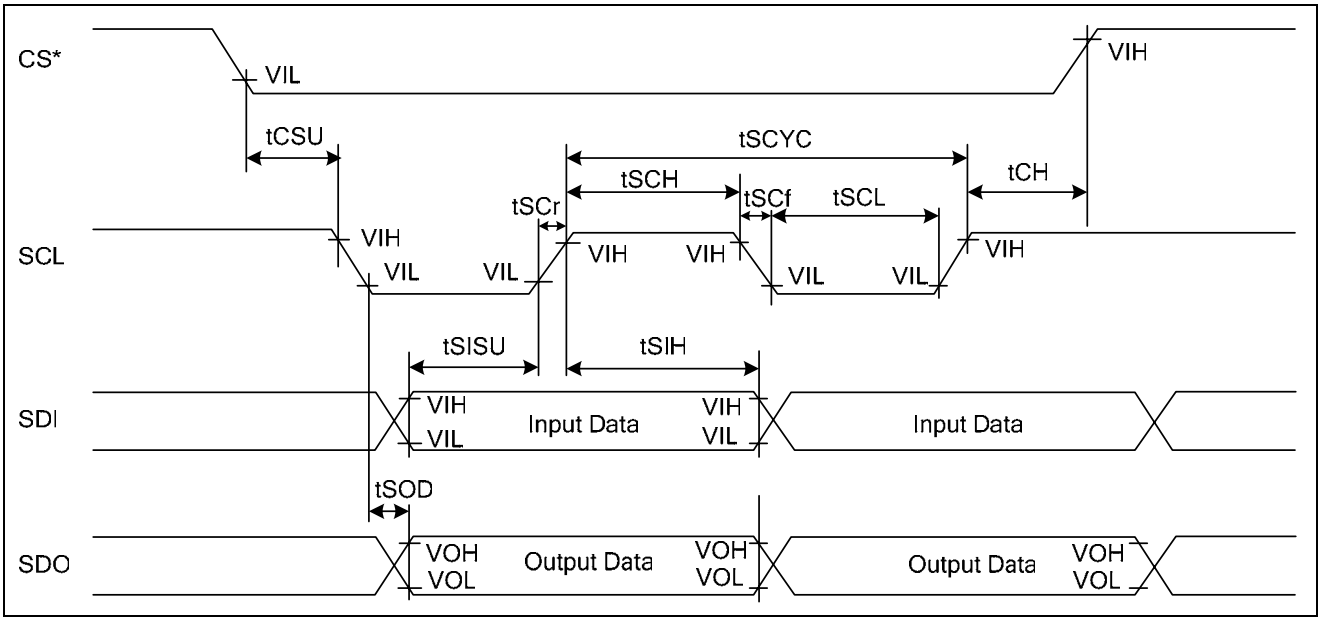


Figure 12-2 SPI interface Timing Diagram

12.3.4. Reset Timing Characteristics (IOVCC=1.65~3.30V)

Table 12-6

Item	Symbol	Unit	Min.	Typ.	Max.
Reset low-level width	tRES	ms	1	–	–
Reset rise time	trRES	μs	–	–	10

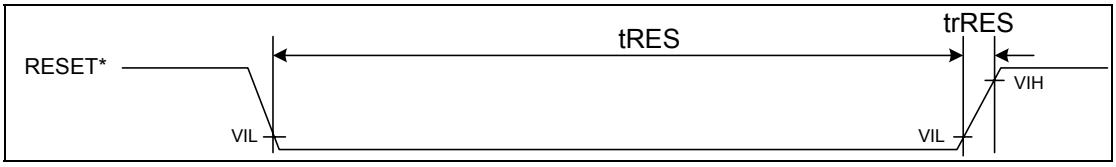


Figure 12-3 Reset Operation

12.3.5. RGB Interface Timing Characteristics

18-/ 16- bit RGB interface, IOVCC=1.65~3.30V

Table 12-7

Item	Symbol	Unit	Min.	Typ.	Max.
VSYNC/HSYNC Setup time	tSYNCS	clock	0	-	1
ENABLE Setup time	tENS	ns	10	-	-
ENABLE Hold time	tENH	ns	20	-	-
DOTCLK low-level pulse width	PWDL	ns	40	-	-
DOTCLK high-level pulse width	PWDH	ns	40	-	-
DOTCLK cycle time	tCYCD	ns	100	-	-
Data setup time	tPDS	ns	10	-	-
Data hold time	tPDH	ns	40	-	-
DOTCLK, VSYNC and HSYNC rise/fall time	trgbr trgbf	ns	-	-	25

6-bit RGB interface, IOVCC=1.65~3.30V

Table 12-8

Item	Symbol	Unit	Min.	Typ.	Max.
VSYNC/HSYNC setup time	tSYNCS	clock	0	-	1
ENABLE setup time	tENS	ns	10	-	-
ENABLE hold time	tENH	ns	25	-	-
DOTCLK low-level pulse width	PWDL	ns	25	-	-
DOTCLK high-level pulse width	PWDH	ns	25	-	-
DOTCLK cycle time	tCYCD	ns	60	-	-
Data setup-time	tPDS	ns	10	-	-
Data hold time	tPDH	ns	25	-	-
DOTCLK, VSYNC, and HSYNC rise/fall time	trgb ttrgbf	ns	-	-	25

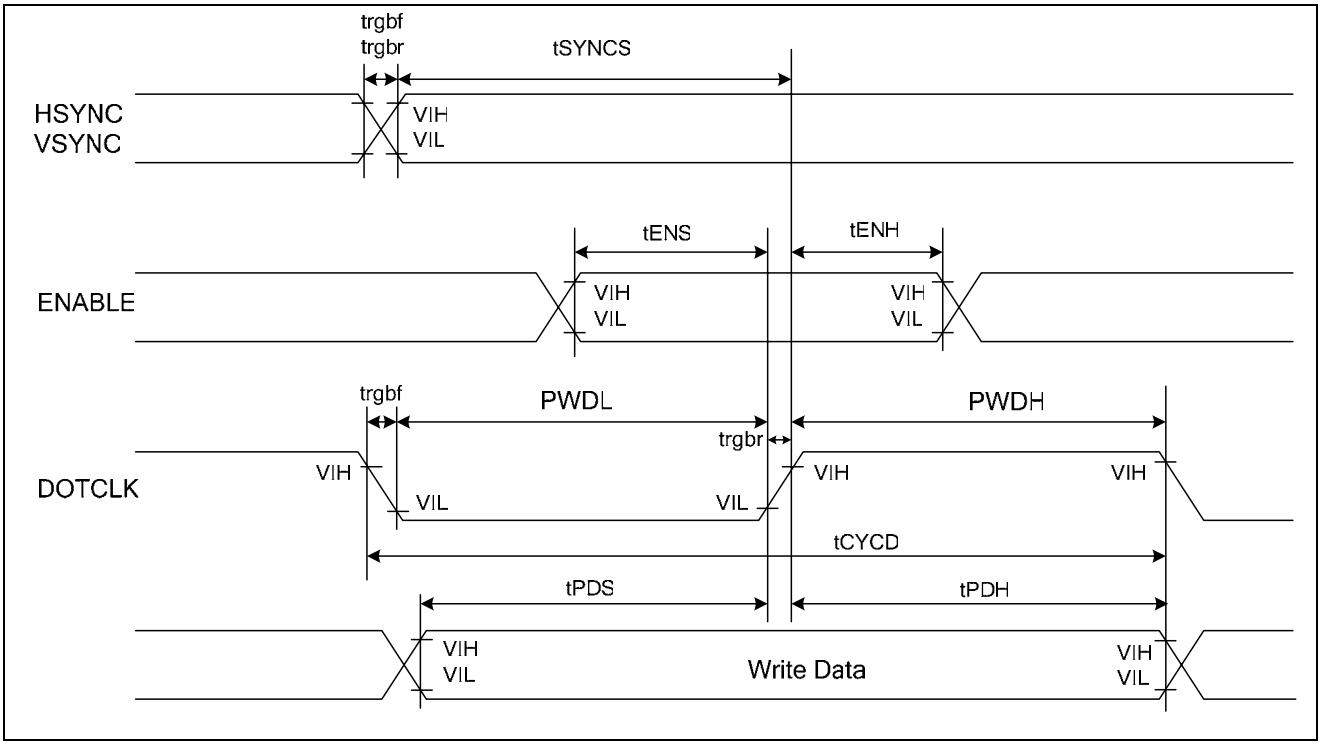
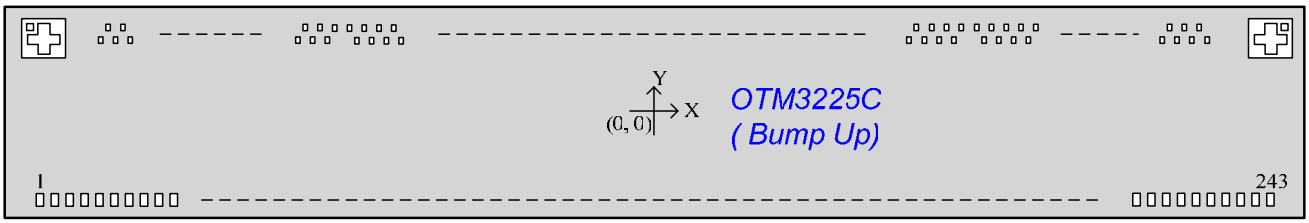


Figure 12-4 RGB interface AC timing Diagram

13. CHIP INFORMATION

13.1. PAD Assignment



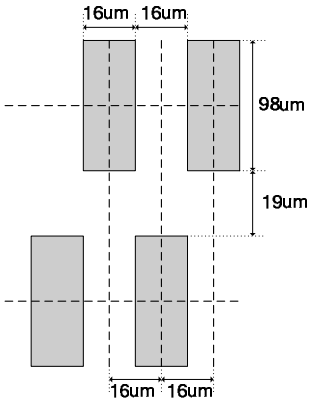
13.2. PAD Dimension

Item	PAD No.	Size		Unit
		X	Y	
Chip Size	-	17820	730	μm
Chip thickness	-	400 ± 20		
Pad pitch	1~243	70	-	
	244~1291	16	-	
Pad size	1~243	50	80	
	244~1291	16	98	

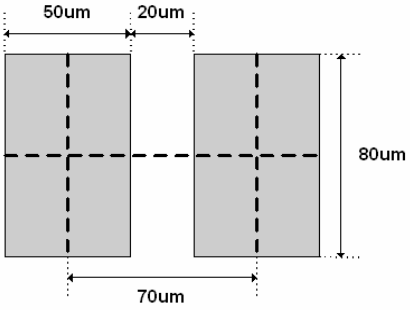
Note1: Chip size included scribe line.

Note2: The Chip thickness is an average value. Please refer to ISO document to get the specific Chip thickness information.

13.2.1. Output Pads



13.2.2. Input Pads



13.3. PAD Locations

PAD No.	Pad Name	X	Y
1	DUMMY1	-8608	-252
2	TEST1	-8538	-252
3	IOGNDDUM	-8468	-252
4	LEDPWM/ TESTO1	-8398	-252
5	LEDON/ TESTO2	-8329	-252
6	TESTO3	-8259	-252
7	IM0_ID	-8189	-252
8	IM1	-8119	-252
9	IM2	-8049	-252
10	IM3	-7979	-252
11	TEST2	-7909	-252
12	TESTO4	-7839	-252
13	TESTO5	-7769	-252
14	TESTO6	-7699	-252
15	TESTO7	-7629	-252
16	TESTO8	-7559	-252
17	TESTO9	-7489	-252
18	TESTO10	-7419	-252
19	RESET	-7349	-252
20	RESET	-7279	-252
21	VSYNC	-7209	-252
22	HSYNC	-7139	-252
23	DOTCLK	-7069	-252
24	ENABLE	-6999	-252
25	DB17	-6904	-252
26	DB16	-6824	-252
27	DB15	-6744	-252
28	DB14	-6664	-252
29	DB13	-6584	-252
30	TESTO11	-6494	-252
31	DB12	-6404	-252
32	DB11	-6324	-252
33	DB10	-6244	-252
34	DB9	-6164	-252
35	DB8	-6084	-252
36	TEST3	-5989	-252
37	TESTO12	-5919	-252
38	DB7	-5824	-252
39	DB6	-5744	-252
40	DB5	-5664	-252
41	DB4	-5584	-252
42	DB3	-5504	-252
43	DB2	-5424	-252
44	DB1	-5344	-252
45	DB0	-5264	-252
46	TESTO13	-5179	-252
47	SDO	-5109	-252
48	SDI	-5039	-252
49	RD	-4969	-252
50	WR_SCL	-4899	-252
51	RS	-4829	-252
52	CS	-4759	-252
53	TESTO14	-4689	-252
54	TESTO15	-4619	-252
55	FMARK	-4549	-252
56	TESTO16	-4479	-252
57	TS8	-4409	-252
58	TS7	-4339	-252
59	TS6	-4269	-252
60	TS5	-4199	-252
61	TS4	-4129	-252
62	TS3	-4059	-252
63	TS2	-3989	-252
64	TS1	-3919	-252
65	TS0	-3849	-252
66	DUMMY2	-3779	-252
67	IOVCC	-3709	-252
68	IOVCC	-3639	-252
69	IOVCC	-3569	-252
70	IOVCC	-3499	-252
71	IOVCC	-3429	-252
72	IOVCC	-3359	-252
73	VDDD	-3289	-252
74	VDDD	-3219	-252
75	VDDD	-3149	-252
76	VDDD	-3079	-252
77	VDDD	-3009	-252
78	VDDD	-2939	-252
79	VDDD	-2869	-252
80	VDDD	-2800	-252
81	VDDD	-2730	-252
82	VDDD	-2660	-252
83	VDDD	-2590	-252
84	DUMMY3	-2520	-252
85	GND	-2450	-252
86	GND	-2380	-252
87	GND	-2310	-252
88	GND	-2240	-252
89	GND	-2170	-252
90	GND	-2100	-252
91	GND	-2030	-252
92	GND	-1960	-252
93	VGS	-1890	-252
94	VGS	-1820	-252
95	RGND	-1750	-252
96	RGND	-1680	-252
97	RGND	-1610	-252
98	RGND	-1540	-252
99	RGND	-1470	-252
100	AGND	-1400	-252
101	AGND	-1330	-252
102	AGND	-1260	-252
103	AGND	-1190	-252
104	AGND	-1120	-252
105	DUMMY4	-1050	-252
106	DUMMY5	-980	-252
107	DUMMY6	-910	-252
108	VCOM	-840	-252
109	VCOM	-770	-252
110	VCOM	-700	-252
111	VCOM	-630	-252
112	VCOM	-560	-252
113	VCOM	-490	-252
114	VCOM	-420	-252
115	VCOMH	-350	-252
116	VCOMH	-280	-252
117	VCOMH	-210	-252
118	VCOMH	-140	-252
119	VCOMH	-70	-252
120	VCOMH	0	-252
121	VCOML	70	-252
122	VCOML	140	-252
123	VCOML	210	-252
124	VCOML	280	-252
125	VREG1OUT	350	-252
126	VREG1OUT	420	-252
127	VREG1OUT	490	-252
128	DUMMY7	560	-252
129	DUMMY8	630	-252
130	DUMMY9	700	-252
131	VCL	770	-252
132	VCL	840	-252
133	VCL	910	-252
134	VCL	980	-252
135	VCL	1050	-252
136	DDVDH	1120	-252
137	DDVDH	1190	-252
138	DDVDH	1260	-252
139	DDVDH	1330	-252

PAD No.	Pad Name	X	Y
140	DDVDH	1400	-252
141	DDVDH	1470	-252
142	VCI1	1540	-252
143	VCI1	1610	-252
144	VCI1	1680	-252
145	VCI	1750	-252
146	VCI	1820	-252
147	VCI	1890	-252
148	VCI	1960	-252
149	VCI	2030	-252
150	VCI	2100	-252
151	VCI	2170	-252
152	VCI	2240	-252
153	VCI	2310	-252
154	VCI	2380	-252
155	VCI	2450	-252
156	VCI	2520	-252
157	VCI	2590	-252
158	VCI	2660	-252
159	VCI	2730	-252
160	VCI	2800	-252
161	VCI	2869	-252
162	VCI	2939	-252
163	DUMMY10	3009	-252
164	DUMMY11	3079	-252
165	C12N	3149	-252
166	C12N	3219	-252
167	C12N	3289	-252
168	C12N	3359	-252
169	C12N	3429	-252
170	C12P	3499	-252
171	C12P	3569	-252
172	C12P	3639	-252
173	C12P	3709	-252
174	C12P	3779	-252
175	C11N	3849	-252
176	C11N	3919	-252
177	C11N	3989	-252
178	C11N	4059	-252
179	C11N	4129	-252
180	C11P	4199	-252
181	C11P	4269	-252
182	C11P	4339	-252
183	C11P	4409	-252
184	C11P	4479	-252
185	VGL	4549	-252
186	VGL	4619	-252
187	VGL	4689	-252
188	VGL	4759	-252
189	VGL	4829	-252
190	VGL	4899	-252
191	VGL	4969	-252
192	VGL	5039	-252
193	VGL	5109	-252
194	VGL	5179	-252
195	GND	5249	-252
196	GND	5319	-252
197	GND	5389	-252
198	VGH	5459	-252
199	VGH	5529	-252
200	VGH	5599	-252
201	VGH	5669	-252
202	VGH	5739	-252
203	VGH	5809	-252
204	DUMMY12	5879	-252
205	DUMMY13	5949	-252
206	C13N	6019	-252
207	C13N	6089	-252
208	C13N	6159	-252
209	C13N	6229	-252
210	C13P	6299	-252
211	C13P	6369	-252
212	C13P	6439	-252
213	C13P	6509	-252
214	C21N	6579	-252
215	C21N	6649	-252
216	C21N	6719	-252
217	C21N	6789	-252
218	C21N	6859	-252
219	C21N	6929	-252
220	C21N	6999	-252
221	C21P	7069	-252
222	C21P	7139	-252
223	C21P	7209	-252
224	C21P	7279	-252
225	C21P	7349	-252
226	C21P	7419	-252
227	C21P	7489	-252
228	C22N	7559	-252
229	C22N	7629	-252
230	C22N	7699	-252
231	C22N	7769	-252
232	C22N	7839	-252
233	C22N	7909	-252
234	C22N	7979	-252
235	C22P	8049	-252
236	C22P	8119	-252
237	C22P	8189	-252
238	C22P	8259	-252
239	C22P	8329	-252
240	C22P	8398	-252
241	C22P	8468	-252
242	DUMMY14	8538	-252
243	DUMMY15	8608	-252
244	DUMMY20	8657	148
245	G320	8641	265
246	G318	8625	148
247	G316	8609	265
248	G314	8593	148
249	G312	8577	265
250	G310	8561	148
251	G308	8545	265
252	G306	8529	148
253	G304	8513	265
254	G302	8497	148
255	G300	8481	265
256	G298	8465	148
257	G296	8449	265
258	G294	8433	148
259	G292	8417	265
260	G290	8401	148
261	G288	8385	265
262	G286	8369	148
263	G284	8354	265
264	G282	8338	148
265	G280	8322	265
266	G278	8306	148
267	G276	8290	265
268	G274	8274	148
269	G272	8258	265
270	G270	8242	148
271	G268	8226	265
272	G266	8210	148
273	G264	8194	265
274	G262	8178	148
275	G260	8162	265
276	G258	8146	148
277	G256	8130	265
278	G254	8114	148
279	G252	8098	265
280	G250	8082	148
281	G248	8066	265
282	G246	8050	148
283	G244	8034	265
284	G242	8018	148
285	G240	8002	265
286	G238	7986	148

PAD No.	Pad Name	X	Y
287	G236	7970	265
288	G234	7954	148
289	G232	7938	265
290	G230	7922	148
291	G228	7906	265
292	G226	7890	148
293	G224	7874	265
294	G222	7858	148
295	G220	7842	265
296	G218	7826	148
297	G216	7810	265
298	G214	7794	148
299	G212	7778	265
300	G210	7762	148
301	G208	7746	265
302	G206	7730	148
303	G204	7714	265
304	G202	7698	148
305	G200	7682	265
306	G198	7666	148
307	G196	7650	265
308	G194	7634	148
309	G192	7618	265
310	G190	7602	148
311	G188	7586	265
312	G186	7570	148
313	G184	7554	265
314	G182	7538	148
315	G180	7522	265
316	G178	7506	148
317	G176	7490	265
318	G174	7474	148
319	G172	7458	265
320	G170	7442	148
321	G168	7426	265
322	G166	7410	148
323	G164	7394	265
324	G162	7378	148
325	G160	7362	265
326	G158	7346	148
327	G156	7330	265
328	G154	7314	148
329	G152	7298	265
330	G150	7282	148
331	G148	7266	265
332	G146	7250	148
333	G144	7234	265
334	G142	7218	148
335	G140	7202	265
336	G138	7186	148
337	G136	7170	265
338	G134	7154	148
339	G132	7138	265
340	G130	7122	148
341	G128	7106	265
342	G126	7090	148
343	G124	7074	265
344	G122	7058	148
345	G120	7042	265
346	G118	7026	148
347	G116	7010	265
348	G114	6994	148
349	G112	6978	265
350	G110	6962	148
351	G108	6946	265
352	G106	6930	148
353	G104	6914	265
354	G102	6898	148
355	G100	6882	265
356	G98	6866	148
357	G96	6850	265
358	G94	6834	148
359	G92	6818	265
360	G90	6802	148
361	G88	6786	265
362	G86	6770	148
363	G84	6754	265
364	G82	6738	148
365	G80	6722	265
366	G78	6706	148
367	G76	6690	265
368	G74	6674	148
369	G72	6658	265
370	G70	6642	148
371	G68	6626	265
372	G66	6610	148
373	G64	6594	265
374	G62	6578	148
375	G60	6562	265
376	G58	6546	148
377	G56	6530	265
378	G54	6514	148
379	G52	6498	265
380	G50	6482	148
381	G48	6466	265
382	G46	6450	148
383	G44	6434	265
384	G42	6418	148
385	G40	6402	265
386	G38	6386	148
387	G36	6370	265
388	G34	6354	148
389	G32	6338	265
390	G30	6322	148
391	G28	6306	265
392	G26	6290	148
393	G24	6274	265
394	G22	6258	148
395	G20	6242	265
396	G18	6226	148
397	G16	6210	265
398	G14	6194	148
399	G12	6178	265
400	G10	6162	148
401	G8	6146	265
402	G6	6130	148
403	G4	6114	265
404	G2	6098	148
405	DUMMY21	6082	265
406	DUMMY22	6046	265
407	S720	6030	148
408	S719	6014	265
409	S718	5998	148
410	S717	5982	265
411	S716	5966	148
412	S715	5950	265
413	S714	5934	148
414	S713	5918	265
415	S712	5902	148
416	S711	5886	265
417	S710	5870	148
418	S709	5854	265
419	S708	5838	148
420	S707	5822	265
421	S706	5806	148
422	S705	5790	265
423	S704	5774	148
424	S703	5758	265
425	S702	5742	148
426	S701	5726	265
427	S700	5710	148
428	S699	5694	265
429	S698	5678	148
430	S697	5662	265
431	S696	5646	148
432	S695	5630	265
433	S694	5614	148

PAD No.	Pad Name	X	Y
434	S693	5598	265
435	S692	5582	148
436	S691	5566	265
437	S690	5550	148
438	S689	5534	265
439	S688	5518	148
440	S687	5502	265
441	S686	5486	148
442	S685	5470	265
443	S684	5454	148
444	S683	5438	265
445	S682	5422	148
446	S681	5406	265
447	S680	5390	148
448	S679	5374	265
449	S678	5358	148
450	S677	5342	265
451	S676	5326	148
452	S675	5310	265
453	S674	5294	148
454	S673	5278	265
455	S672	5262	148
456	S671	5246	265
457	S670	5230	148
458	S669	5214	265
459	S668	5198	148
460	S667	5182	265
461	S666	5166	148
462	S665	5150	265
463	S664	5134	148
464	S663	5118	265
465	S662	5102	148
466	S661	5086	265
467	S660	5070	148
468	S659	5054	265
469	S658	5038	148
470	S657	5022	265
471	S656	5006	148
472	S655	4990	265
473	S654	4974	148
474	S653	4958	265
475	S652	4942	148
476	S651	4926	265
477	S650	4910	148
478	S649	4894	265
479	S648	4878	148
480	S647	4862	265
481	S646	4846	148
482	S645	4830	265

PAD No.	Pad Name	X	Y
483	S644	4814	148
484	S643	4798	265
485	S642	4782	148
486	S641	4766	265
487	S640	4750	148
488	S639	4734	265
489	S638	4718	148
490	S637	4702	265
491	S636	4686	148
492	S635	4670	265
493	S634	4654	148
494	S633	4638	265
495	S632	4622	148
496	S631	4606	265
497	S630	4590	148
498	S629	4574	265
499	S628	4558	148
500	S627	4542	265
501	S626	4526	148
502	S625	4510	265
503	S624	4494	148
504	S623	4478	265
505	S622	4462	148
506	S621	4446	265
507	S620	4430	148
508	S619	4414	265
509	S618	4398	148
510	S617	4382	265
511	S616	4366	148
512	S615	4350	265
513	S614	4334	148
514	S613	4318	265
515	S612	4302	148
516	S611	4286	265
517	S610	4270	148
518	S609	4254	265
519	S608	4238	148
520	S607	4222	265
521	S606	4206	148
522	S605	4190	265
523	S604	4174	148
524	S603	4158	265
525	S602	4142	148
526	S601	4126	265
527	S600	4110	148
528	S599	4094	265
529	S598	4078	148
530	S597	4062	265
531	S596	4046	148

PAD No.	Pad Name	X	Y
532	S595	4030	265
533	S594	4014	148
534	S593	3998	265
535	S592	3982	148
536	S591	3966	265
537	S590	3950	148
538	S589	3934	265
539	S588	3918	148
540	S587	3902	265
541	S586	3886	148
542	S585	3870	265
543	S584	3854	148
544	S583	3838	265
545	S582	3822	148
546	S581	3806	265
547	S580	3790	148
548	S579	3774	265
549	S578	3758	148
550	S577	3742	265
551	S576	3726	148
552	S575	3710	265
553	S574	3694	148
554	S573	3678	265
555	S572	3662	148
556	S571	3646	265
557	S570	3630	148
558	S569	3614	265
559	S568	3598	148
560	S567	3582	265
561	S566	3566	148
562	S565	3550	265
563	S564	3534	148
564	S563	3518	265
565	S562	3502	148
566	S561	3486	265
567	S560	3470	148
568	S559	3454	265
569	S558	3438	148
570	S557	3422	265
571	S556	3406	148
572	S555	3390	265
573	S554	3374	148
574	S553	3358	265
575	S552	3342	148
576	S551	3326	265
577	S550	3310	148
578	S549	3294	265
579	S548	3278	148
580	S547	3262	265

PAD No.	Pad Name	X	Y
581	S546	3246	148
582	S545	3230	265
583	S544	3214	148
584	S543	3198	265
585	S542	3182	148
586	S541	3166	265
587	S540	3150	148
588	S539	3134	265
589	S538	3118	148
590	S537	3102	265
591	S536	3086	148
592	S535	3070	265
593	S534	3054	148
594	S533	3038	265
595	S532	3022	148
596	S531	3006	265
597	S530	2990	148
598	S529	2974	265
599	S528	2958	148
600	S527	2942	265
601	S526	2926	148
602	S525	2910	265
603	S524	2894	148
604	S523	2878	265
605	S522	2862	148
606	S521	2846	265
607	S520	2830	148
608	S519	2814	265
609	S518	2799	148
610	S517	2783	265
611	S516	2767	148
612	S515	2751	265
613	S514	2735	148
614	S513	2719	265
615	S512	2703	148
616	S511	2687	265
617	S510	2671	148
618	S509	2655	265
619	S508	2639	148
620	S507	2623	265
621	S506	2607	148
622	S505	2591	265
623	S504	2575	148
624	S503	2559	265
625	S502	2543	148
626	S501	2527	265
627	S500	2511	148
628	S499	2495	265
629	S498	2479	148

PAD No.	Pad Name	X	Y
630	S497	2463	265
631	S496	2447	148
632	S495	2431	265
633	S494	2415	148
634	S493	2399	265
635	S492	2383	148
636	S491	2367	265
637	S490	2351	148
638	S489	2335	265
639	S488	2319	148
640	S487	2303	265
641	S486	2287	148
642	S485	2271	265
643	S484	2255	148
644	S483	2239	265
645	S482	2223	148
646	S481	2207	265
647	S480	2191	148
648	S479	2175	265
649	S478	2159	148
650	S477	2143	265
651	S476	2127	148
652	S475	2111	265
653	S474	2095	148
654	S473	2079	265
655	S472	2063	148
656	S471	2047	265
657	S470	2031	148
658	S469	2015	265
659	S468	1999	148
660	S467	1983	265
661	S466	1967	148
662	S465	1951	265
663	S464	1935	148
664	S463	1919	265
665	S462	1903	148
666	S461	1887	265
667	S460	1871	148
668	S459	1855	265
669	S458	1839	148
670	S457	1823	265
671	S456	1807	148
672	S455	1791	265
673	S454	1775	148
674	S453	1759	265
675	S452	1743	148
676	S451	1727	265
677	S450	1711	148
678	S449	1695	265

PAD No.	Pad Name	X	Y
679	S448	1679	148
680	S447	1663	265
681	S446	1647	148
682	S445	1631	265
683	S444	1615	148
684	S443	1599	265
685	S442	1583	148
686	S441	1567	265
687	S440	1551	148
688	S439	1535	265
689	S438	1519	148
690	S437	1503	265
691	S436	1487	148
692	S435	1471	265
693	S434	1455	148
694	S433	1439	265
695	S432	1423	148
696	S431	1407	265
697	S430	1391	148
698	S429	1375	265
699	S428	1359	148
700	S427	1343	265
701	S426	1327	148
702	S425	1311	265
703	S424	1295	148
704	S423	1279	265
705	S422	1263	148
706	S421	1247	265
707	S420	1231	148
708	S419	1215	265
709	S418	1199	148
710	S417	1183	265
711	S416	1167	148
712	S415	1151	265
713	S414	1135	148
714	S413	1119	265
715	S412	1103	148
716	S411	1087	265
717	S410	1071	148
718	S409	1055	265
719	S408	1039	148
720	S407	1023	265
721	S406	1007	148
722	S405	991	265
723	S404	975	148
724	S403	959	265
725	S402	943	148
726	S401	927	265
727	S400	911	148

PAD No.	Pad Name	X	Y
728	S399	895	265
729	S398	879	148
730	S397	863	265
731	S396	847	148
732	S395	831	265
733	S394	815	148
734	S393	799	265
735	S392	783	148
736	S391	767	265
737	S390	751	148
738	S389	735	265
739	S388	719	148
740	S387	703	265
741	S386	687	148
742	S385	671	265
743	S384	655	148
744	S383	639	265
745	S382	623	148
746	S381	607	265
747	S380	591	148
748	S379	575	265
749	S378	559	148
750	S377	543	265
751	S376	527	148
752	S375	511	265
753	S374	495	148
754	S373	479	265
755	S372	463	148
756	S371	447	265
757	S370	431	148
758	S369	415	265
759	S368	399	148
760	S367	383	265
761	S366	367	148
762	S365	351	265
763	S364	335	148
764	S363	319	265
765	S362	303	148
766	S361	287	265
767	DUMMY23	271	148
768	DUMMY24	-271	148
769	S360	-287	265
770	S359	-303	148
771	S358	-319	265
772	S357	-335	148
773	S356	-351	265
774	S355	-367	148
775	S354	-383	265
776	S353	-399	148

PAD No.	Pad Name	X	Y
777	S352	-415	265
778	S351	-431	148
779	S350	-447	265
780	S349	-463	148
781	S348	-479	265
782	S347	-495	148
783	S346	-511	265
784	S345	-527	148
785	S344	-543	265
786	S343	-559	148
787	S342	-575	265
788	S341	-591	148
789	S340	-607	265
790	S339	-623	148
791	S338	-639	265
792	S337	-655	148
793	S336	-671	265
794	S335	-687	148
795	S334	-703	265
796	S333	-719	148
797	S332	-735	265
798	S331	-751	148
799	S330	-767	265
800	S329	-783	148
801	S328	-799	265
802	S327	-815	148
803	S326	-831	265
804	S325	-847	148
805	S324	-863	265
806	S323	-879	148
807	S322	-895	265
808	S321	-911	148
809	S320	-927	265
810	S319	-943	148
811	S318	-959	265
812	S317	-975	148
813	S316	-991	265
814	S315	-1007	148
815	S314	-1023	265
816	S313	-1039	148
817	S312	-1055	265
818	S311	-1071	148
819	S310	-1087	265
820	S309	-1103	148
821	S308	-1119	265
822	S307	-1135	148
823	S306	-1151	265
824	S305	-1167	148
825	S304	-1183	265

PAD No.	Pad Name	X	Y
826	S303	-1199	148
827	S302	-1215	265
828	S301	-1231	148
829	S300	-1247	265
830	S299	-1263	148
831	S298	-1279	265
832	S297	-1295	148
833	S296	-1311	265
834	S295	-1327	148
835	S294	-1343	265
836	S293	-1359	148
837	S292	-1375	265
838	S291	-1391	148
839	S290	-1407	265
840	S289	-1423	148
841	S288	-1439	265
842	S287	-1455	148
843	S286	-1471	265
844	S285	-1487	148
845	S284	-1503	265
846	S283	-1519	148
847	S282	-1535	265
848	S281	-1551	148
849	S280	-1567	265
850	S279	-1583	148
851	S278	-1599	265
852	S277	-1615	148
853	S276	-1631	265
854	S275	-1647	148
855	S274	-1663	265
856	S273	-1679	148
857	S272	-1695	265
858	S271	-1711	148
859	S270	-1727	265
860	S269	-1743	148
861	S268	-1759	265
862	S267	-1775	148
863	S266	-1791	265
864	S265	-1807	148
865	S264	-1823	265
866	S263	-1839	148
867	S262	-1855	265
868	S261	-1871	148
869	S260	-1887	265
870	S259	-1903	148
871	S258	-1919	265
872	S257	-1935	148
873	S256	-1951	265
874	S255	-1967	148

PAD No.	Pad Name	X	Y
875	S254	-1983	265
876	S253	-1999	148
877	S252	-2015	265
878	S251	-2031	148
879	S250	-2047	265
880	S249	-2063	148
881	S248	-2079	265
882	S247	-2095	148
883	S246	-2111	265
884	S245	-2127	148
885	S244	-2143	265
886	S243	-2159	148
887	S242	-2175	265
888	S241	-2191	148
889	S240	-2207	265
890	S239	-2223	148
891	S238	-2239	265
892	S237	-2255	148
893	S236	-2271	265
894	S235	-2287	148
895	S234	-2303	265
896	S233	-2319	148
897	S232	-2335	265
898	S231	-2351	148
899	S230	-2367	265
900	S229	-2383	148
901	S228	-2399	265
902	S227	-2415	148
903	S226	-2431	265
904	S225	-2447	148
905	S224	-2463	265
906	S223	-2479	148
907	S222	-2495	265
908	S221	-2511	148
909	S220	-2527	265
910	S219	-2543	148
911	S218	-2559	265
912	S217	-2575	148
913	S216	-2591	265
914	S215	-2607	148
915	S214	-2623	265
916	S213	-2639	148
917	S212	-2655	265
918	S211	-2671	148
919	S210	-2687	265
920	S209	-2703	148
921	S208	-2719	265
922	S207	-2735	148
923	S206	-2751	265
924	S205	-2767	148
925	S204	-2783	265
926	S203	-2799	148
927	S202	-2814	265
928	S201	-2830	148
929	S200	-2846	265
930	S199	-2862	148
931	S198	-2878	265
932	S197	-2894	148
933	S196	-2910	265
934	S195	-2926	148
935	S194	-2942	265
936	S193	-2958	148
937	S192	-2974	265
938	S191	-2990	148
939	S190	-3006	265
940	S189	-3022	148
941	S188	-3038	265
942	S187	-3054	148
943	S186	-3070	265
944	S185	-3086	148
945	S184	-3102	265
946	S183	-3118	148
947	S182	-3134	265
948	S181	-3150	148
949	S180	-3166	265
950	S179	-3182	148
951	S178	-3198	265
952	S177	-3214	148
953	S176	-3230	265
954	S175	-3246	148
955	S174	-3262	265
956	S173	-3278	148
957	S172	-3294	265
958	S171	-3310	148
959	S170	-3326	265
960	S169	-3342	148
961	S168	-3358	265
962	S167	-3374	148
963	S166	-3390	265
964	S165	-3406	148
965	S164	-3422	265
966	S163	-3438	148
967	S162	-3454	265
968	S161	-3470	148
969	S160	-3486	265
970	S159	-3502	148
971	S158	-3518	265
972	S157	-3534	148
973	S156	-3550	265
974	S155	-3566	148
975	S154	-3582	265
976	S153	-3598	148
977	S152	-3614	265
978	S151	-3630	148
979	S150	-3646	265
980	S149	-3662	148
981	S148	-3678	265
982	S147	-3694	148
983	S146	-3710	265
984	S145	-3726	148
985	S144	-3742	265
986	S143	-3758	148
987	S142	-3774	265
988	S141	-3790	148
989	S140	-3806	265
990	S139	-3822	148
991	S138	-3838	265
992	S137	-3854	148
993	S136	-3870	265
994	S135	-3886	148
995	S134	-3902	265
996	S133	-3918	148
997	S132	-3934	265
998	S131	-3950	148
999	S130	-3966	265
1000	S129	-3982	148
1001	S128	-3998	265
1002	S127	-4014	148
1003	S126	-4030	265
1004	S125	-4046	148
1005	S124	-4062	265
1006	S123	-4078	148
1007	S122	-4094	265
1008	S121	-4110	148
1009	S120	-4126	265
1010	S119	-4142	148
1011	S118	-4158	265
1012	S117	-4174	148
1013	S116	-4190	265
1014	S115	-4206	148
1015	S114	-4222	265
1016	S113	-4238	148
1017	S112	-4254	265
1018	S111	-4270	148
1019	S110	-4286	265
1020	S109	-4302	148
1021	S108	-4318	265

PAD No.	Pad Name	X	Y
1022	S107	-4334	148
1023	S106	-4350	265
1024	S105	-4366	148
1025	S104	-4382	265
1026	S103	-4398	148
1027	S102	-4414	265
1028	S101	-4430	148
1029	S100	-4446	265
1030	S99	-4462	148
1031	S98	-4478	265
1032	S97	-4494	148
1033	S96	-4510	265
1034	S95	-4526	148
1035	S94	-4542	265
1036	S93	-4558	148
1037	S92	-4574	265
1038	S91	-4590	148
1039	S90	-4606	265
1040	S89	-4622	148
1041	S88	-4638	265
1042	S87	-4654	148
1043	S86	-4670	265
1044	S85	-4686	148
1045	S84	-4702	265
1046	S83	-4718	148
1047	S82	-4734	265
1048	S81	-4750	148
1049	S80	-4766	265
1050	S79	-4782	148
1051	S78	-4798	265
1052	S77	-4814	148
1053	S76	-4830	265
1054	S75	-4846	148
1055	S74	-4862	265
1056	S73	-4878	148
1057	S72	-4894	265
1058	S71	-4910	148
1059	S70	-4926	265
1060	S69	-4942	148
1061	S68	-4958	265
1062	S67	-4974	148
1063	S66	-4990	265
1064	S65	-5006	148
1065	S64	-5022	265
1066	S63	-5038	148
1067	S62	-5054	265
1068	S61	-5070	148
1069	S60	-5086	265
1070	S59	-5102	148

PAD No.	Pad Name	X	Y
1071	S58	-5118	265
1072	S57	-5134	148
1073	S56	-5150	265
1074	S55	-5166	148
1075	S54	-5182	265
1076	S53	-5198	148
1077	S52	-5214	265
1078	S51	-5230	148
1079	S50	-5246	265
1080	S49	-5262	148
1081	S48	-5278	265
1082	S47	-5294	148
1083	S46	-5310	265
1084	S45	-5326	148
1085	S44	-5342	265
1086	S43	-5358	148
1087	S42	-5374	265
1088	S41	-5390	148
1089	S40	-5406	265
1090	S39	-5422	148
1091	S38	-5438	265
1092	S37	-5454	148
1093	S36	-5470	265
1094	S35	-5486	148
1095	S34	-5502	265
1096	S33	-5518	148
1097	S32	-5534	265
1098	S31	-5550	148
1099	S30	-5566	265
1100	S29	-5582	148
1101	S28	-5598	265
1102	S27	-5614	148
1103	S26	-5630	265
1104	S25	-5646	148
1105	S24	-5662	265
1106	S23	-5678	148
1107	S22	-5694	265
1108	S21	-5710	148
1109	S20	-5726	265
1110	S19	-5742	148
1111	S18	-5758	265
1112	S17	-5774	148
1113	S16	-5790	265
1114	S15	-5806	148
1115	S14	-5822	265
1116	S13	-5838	148
1117	S12	-5854	265
1118	S11	-5870	148
1119	S10	-5886	265

PAD No.	Pad Name	X	Y
1120	S9	-5902	148
1121	S8	-5918	265
1122	S7	-5934	148
1123	S6	-5950	265
1124	S5	-5966	148
1125	S4	-5982	265
1126	S3	-5998	148
1127	S2	-6014	265
1128	S1	-6030	148
1129	DUMMY25	-6046	265
1130	DUMMY26	-6082	265
1131	G1	-6098	148
1132	G3	-6114	265
1133	G5	-6130	148
1134	G7	-6146	265
1135	G9	-6162	148
1136	G11	-6178	265
1137	G13	-6194	148
1138	G15	-6210	265
1139	G17	-6226	148
1140	G19	-6242	265
1141	G21	-6258	148
1142	G23	-6274	265
1143	G25	-6290	148
1144	G27	-6306	265
1145	G29	-6322	148
1146	G31	-6338	265
1147	G33	-6354	148
1148	G35	-6370	265
1149	G37	-6386	148
1150	G39	-6402	265
1151	G41	-6418	148
1152	G43	-6434	265
1153	G45	-6450	148
1154	G47	-6466	265
1155	G49	-6482	148
1156	G51	-6498	265
1157	G53	-6514	148
1158	G55	-6530	265
1159	G57	-6546	148
1160	G59	-6562	265
1161	G61	-6578	148
1162	G63	-6594	265
1163	G65	-6610	148
1164	G67	-6626	265
1165	G69	-6642	148
1166	G71	-6658	265
1167	G73	-6674	148
1168	G75	-6690	265

PAD No.	Pad Name	X	Y
1169	G77	-6706	148
1170	G79	-6722	265
1171	G81	-6738	148
1172	G83	-6754	265
1173	G85	-6770	148
1174	G87	-6786	265
1175	G89	-6802	148
1176	G91	-6818	265
1177	G93	-6834	148
1178	G95	-6850	265
1179	G97	-6866	148
1180	G99	-6882	265
1181	G101	-6898	148
1182	G103	-6914	265
1183	G105	-6930	148
1184	G107	-6946	265
1185	G109	-6962	148
1186	G111	-6978	265
1187	G113	-6994	148
1188	G115	-7010	265
1189	G117	-7026	148
1190	G119	-7042	265
1191	G121	-7058	148
1192	G123	-7074	265
1193	G125	-7090	148
1194	G127	-7106	265
1195	G129	-7122	148
1196	G131	-7138	265
1197	G133	-7154	148
1198	G135	-7170	265
1199	G137	-7186	148
1200	G139	-7202	265
1201	G141	-7218	148
1202	G143	-7234	265
1203	G145	-7250	148
1204	G147	-7266	265
1205	G149	-7282	148
1206	G151	-7298	265
1207	G153	-7314	148
1208	G155	-7330	265
1209	G157	-7346	148
1210	G159	-7362	265

PAD No.	Pad Name	X	Y
1211	G161	-7378	148
1212	G163	-7394	265
1213	G165	-7410	148
1214	G167	-7426	265
1215	G169	-7442	148
1216	G171	-7458	265
1217	G173	-7474	148
1218	G175	-7490	265
1219	G177	-7506	148
1220	G179	-7522	265
1221	G181	-7538	148
1222	G183	-7554	265
1223	G185	-7570	148
1224	G187	-7586	265
1225	G189	-7602	148
1226	G191	-7618	265
1227	G193	-7634	148
1228	G195	-7650	265
1229	G197	-7666	148
1230	G199	-7682	265
1231	G201	-7698	148
1232	G203	-7714	265
1233	G205	-7730	148
1234	G207	-7746	265
1235	G209	-7762	148
1236	G211	-7778	265
1237	G213	-7794	148
1238	G215	-7810	265
1239	G217	-7826	148
1240	G219	-7842	265
1241	G221	-7858	148
1242	G223	-7874	265
1243	G225	-7890	148
1244	G227	-7906	265
1245	G229	-7922	148
1246	G231	-7938	265
1247	G233	-7954	148
1248	G235	-7970	265
1249	G237	-7986	148
1250	G239	-8002	265
1251	G241	-8018	148
1252	G243	-8034	265

PAD No.	Pad Name	X	Y
1253	G245	-8050	148
1254	G247	-8066	265
1255	G249	-8082	148
1256	G251	-8098	265
1257	G253	-8114	148
1258	G255	-8130	265
1259	G257	-8146	148
1260	G259	-8162	265
1261	G261	-8178	148
1262	G263	-8194	265
1263	G265	-8210	148
1264	G267	-8226	265
1265	G269	-8242	148
1266	G271	-8258	265
1267	G273	-8274	148
1268	G275	-8290	265
1269	G277	-8306	148
1270	G279	-8322	265
1271	G281	-8338	148
1272	G283	-8354	265
1273	G285	-8369	148
1274	G287	-8385	265
1275	G289	-8401	148
1276	G291	-8417	265
1277	G293	-8433	148
1278	G295	-8449	265
1279	G297	-8465	148
1280	G299	-8481	265
1281	G301	-8497	148
1282	G303	-8513	265
1283	G305	-8529	148
1284	G307	-8545	265
1285	G309	-8561	148
1286	G311	-8577	265
1287	G313	-8593	148
1288	G315	-8609	265
1289	G317	-8625	148
1290	G319	-8641	265
1291	DUMMY27	-8657	148

13.4. Alignment Mark

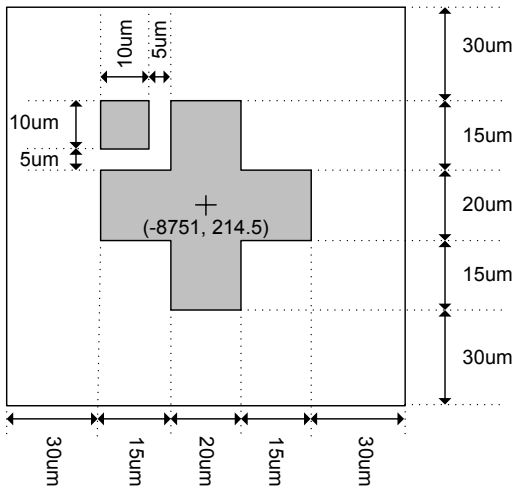
--Alignment Mark coordinate

Left (-8751, 214.5)

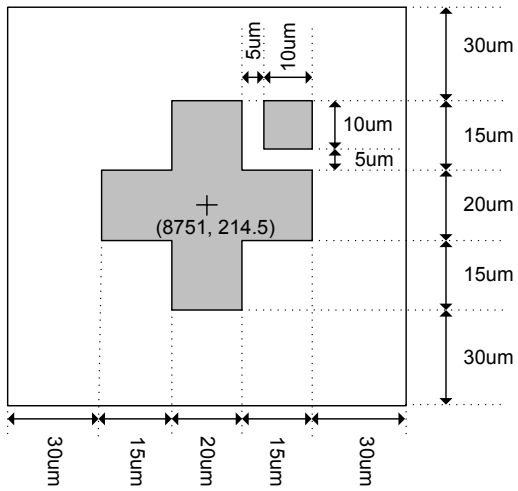
Right (8751, 214.5)

--Alignment Mark size

Left



Right



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15. REVISION HISTORY

Date	Revision #	Description	Page
FEB. 01, 2010	0.5	1. Modify VGL range:	5
		2. Correct type-mistake: (DE) ➔ (ENABLE)	7
		3. /CS pin function: Must connect to the IOVCC level when not used. ➔ Must connect to MPU.	8
		4. LEDPWM & LEDON descriptions:	10
		(a)Modify: Connected with VCI ➔ Connect with LED Driver	10
		(b)Add: Must connect to the GND level or Open (floating) when not in use.	10
		5. Add VGS description: Must connect to the GND level for normal usage.	10
		6. Modify: (RESET*, CS*, WR, RD*) ➔ (/RESET, /CS, /WR, /RD)	10
		7. Correct type-mistake: (Figure 6-1 to Figure 15-5) ➔ (Figure 5-1 to Figure 15-5)	11
		8. Add Instruction Group: CABC Function	11
		9. Modify Figure 5.5 : nCS ➔ /CS	11
		10. Correct Table 5-1:	13~14
		(a)Modify default value of ISC[1:0]: (1,1) ➔ (0,0)	
		(b)Modify name: TRIREG ➔ TRI	
		(b)Modify default value of RTNE[1]: 1 ➔ 0	
		11. Modify description of section 5.2.2.2:	15
		(a) ID Read Register (SR) ➔ Read ID Register	
		(b) RS bit: (0) ➔ (1)	
		(c) IC metal option for customer's ➔ IC metal option or Trim option for customer's	
		12. Modify Figure 5.6: OTM3225A ➔ OTM3225C	15
		13. Correct type-mistake: ever ➔ every	16
		14. Correct type-mistake: Table 5-2 ➔ Figure 5-9 & 5-10.	16
		15. Modify description: (neither 8-bit nor 16-bit) ➔ (18-bit bus width or 9-bit bus width)	17
		16. Add Note: Must set TRI=0, when reading back data from GRAM.	17
		17. Add example pictures of scaling factor.	19
		18. Define RSZ=10: Setting Disable ➔ No Scaling	19
		19. Correct type-mistake: description of D1-0 & COL bits	20
		20. Add COL bit & display mode to Table 5-5 and add detail information	20
		21. Add example picture to introduce Base image & Non-lit & Partial display	20
		22. Remove BP bits & FP bits application limit: make sure ➔ recommend	21
		23. Add "with flicker" notice information in Table 5-11	22
		24. Correct type-mistake in Table 5-9: 19 Frame~31 Frame ➔ 17 Frame~29 Frame	22
		25. Delete some SLP bit description:	26
		In sleep mode, no instruction can be accepted except R11h, R13h, bit 3-0 of R12h and R10h (except SAP2-0). Set STB=0 can exit sleep mode.	
		26. Delete some STB bit description:	26
		Be sure that start oscillation following by 10ms delay should be executed before set STB to "0".	
		27. Modify Figure 5-25 : DB8~DB1 ➔ DB17~DB10	36
		28. Modify Table 5-25 : Modify OSC frequency & Add BP/FP/RTNI condition	40
		29. Modify DIVE bits description:	51
		(a) adjust frame frequency ➔ adjust Source line charge time	
		(b) RGB interface mode ➔ system interface mode	
		30. Modify Table 7-2: DB1 to 0 ➔ - (Note: SPI use SDI & SDO)	59

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		2. Modify CABC command B2, B3, BF function description.	52-53
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